Development of a SiC-Based Electronics Technology for Extreme Environments

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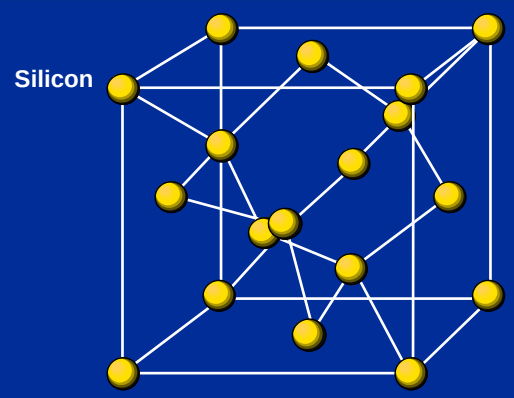
Unique Features of Silicon Carbide

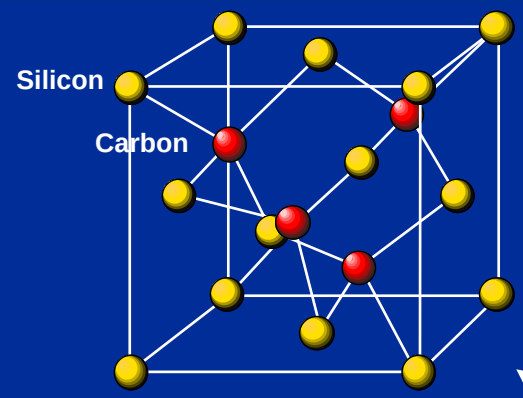
- Consists of an equal number of silicon and carbon atoms, arranged in a hexagonal lattice
- One of the hardest materials known
- Extremely high thermal and chemical stability
- Breakdown field ~ 10x higher than silicon
- Forms a high quality native oxide: SiO_2
- Figure-of-merit for high-frequency power devices is ~ 400x higher than silicon

Crystal Structure of SiC

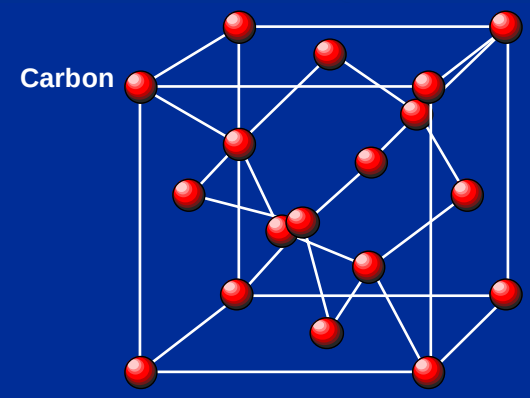
Silicon



Silicon Carbide



Diamond



3C Polytype

4H Polytype
6H Polytype

Electrical Properties

		Silicon	4H-SiC

Temperature Capability

$$J_{LEAKAGE} = \frac{n_i(T)}{\tau_G}$$

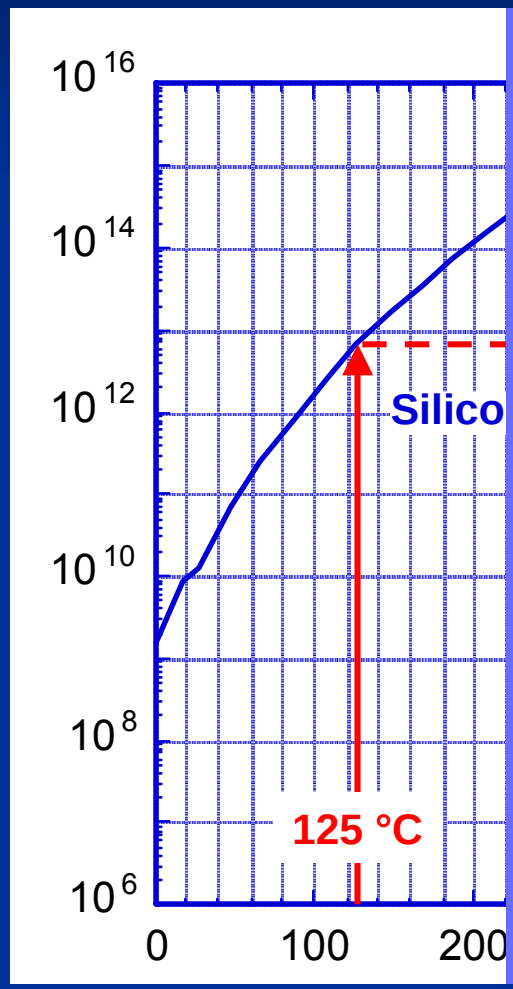
n_i = *Intrinsic Carrier Concentration*

τ_G = *Generation Lifetime*

Temperature Capability

Leakage Current

- τ_G



Limitations Due to Materials Issues

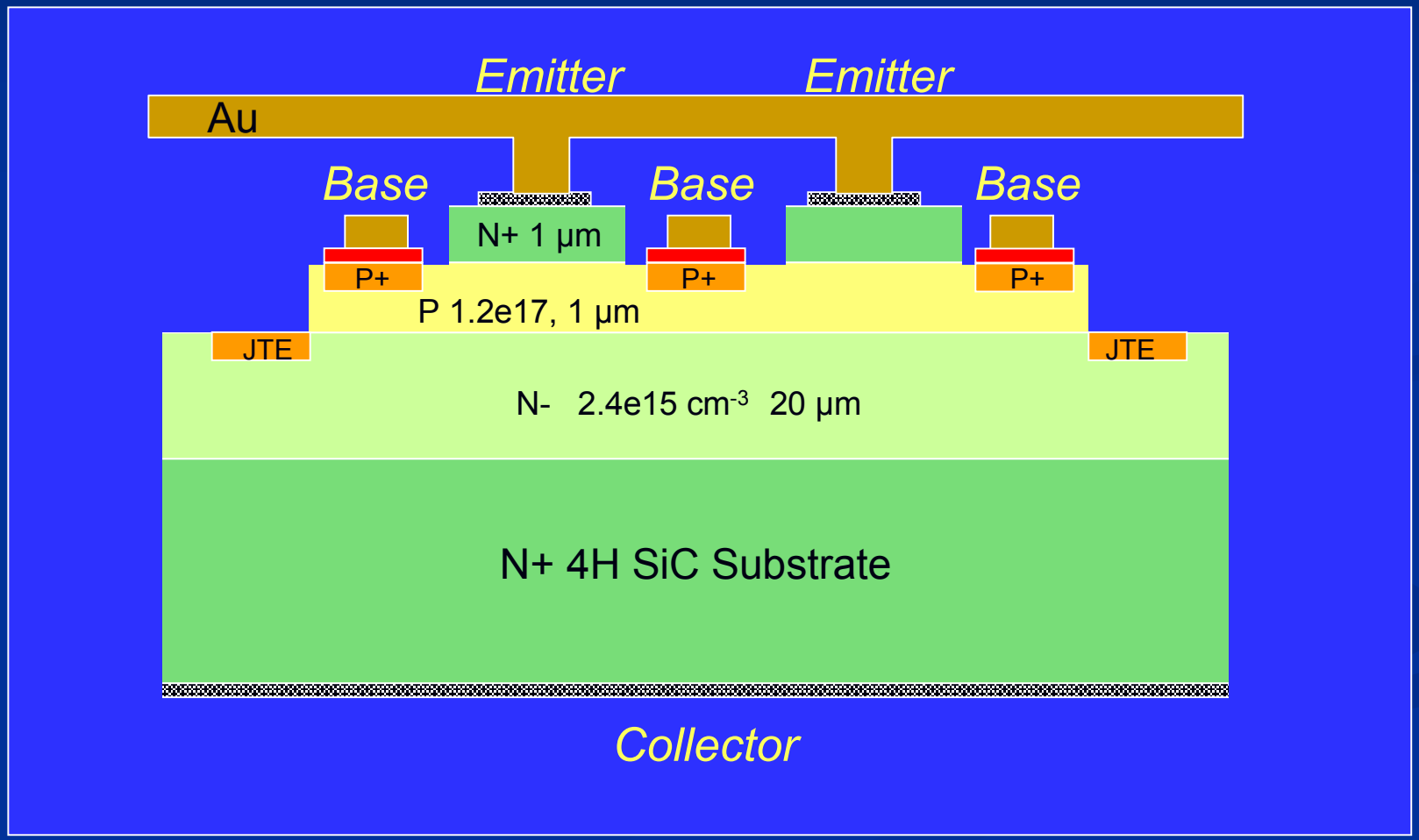
Assumed System Goals

- High Temperature Operation
  - *(≥ 400 °C desired)*
- High Radiation Tolerance
  - *(for use in space applications)*

SiC BJT as Power Switch

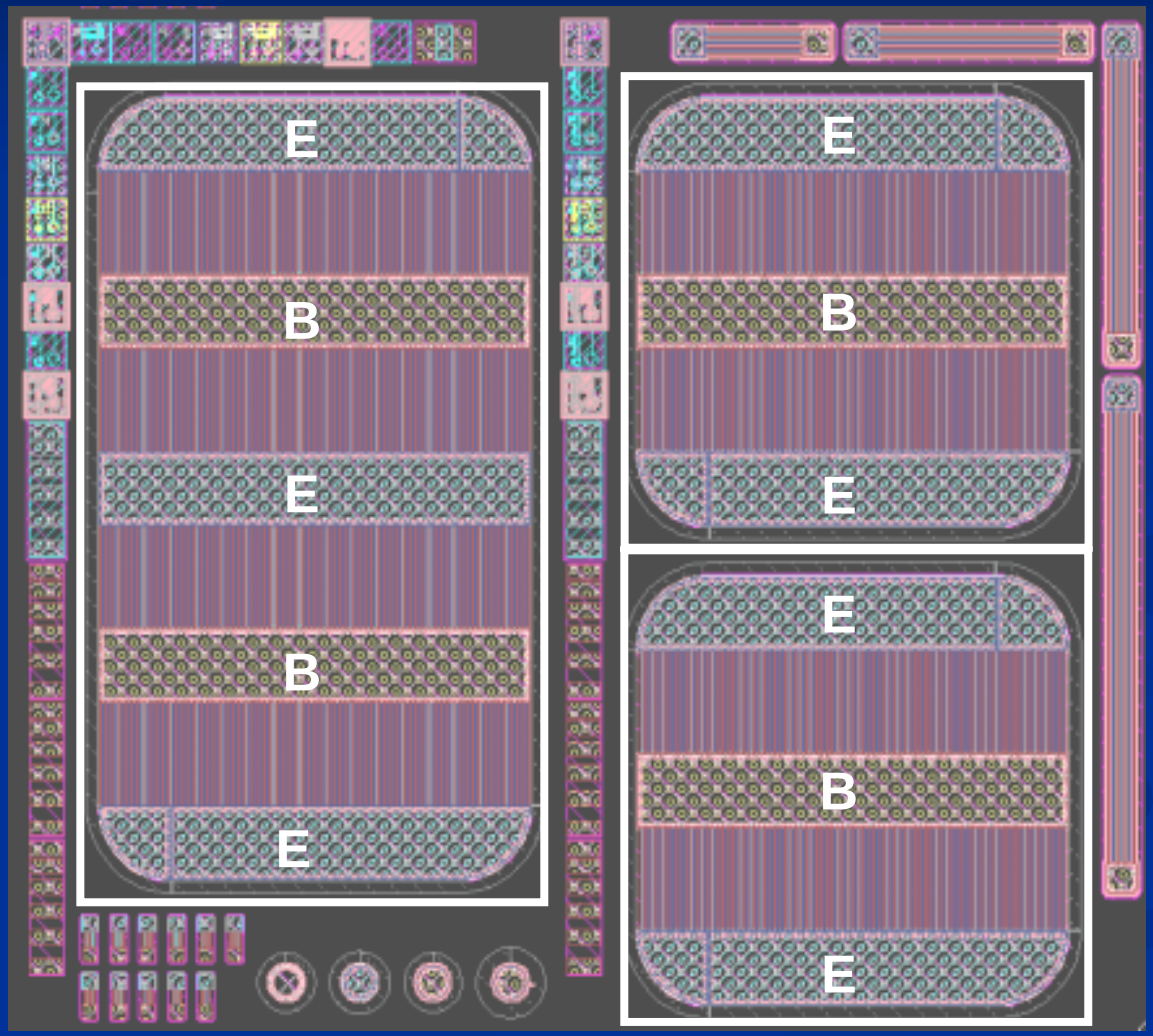
- High Blocking Voltage
  - *(due to high critical field in SiC)*
- High Temperature Operation
  - *(no critical MOS oxide)*
- High Radiation Tolerance
  - *(no critical MOS oxide)*
- Low On-Resistance
  - *(due to conductivity modulation of drift region)*

SiC BJT Fabrication



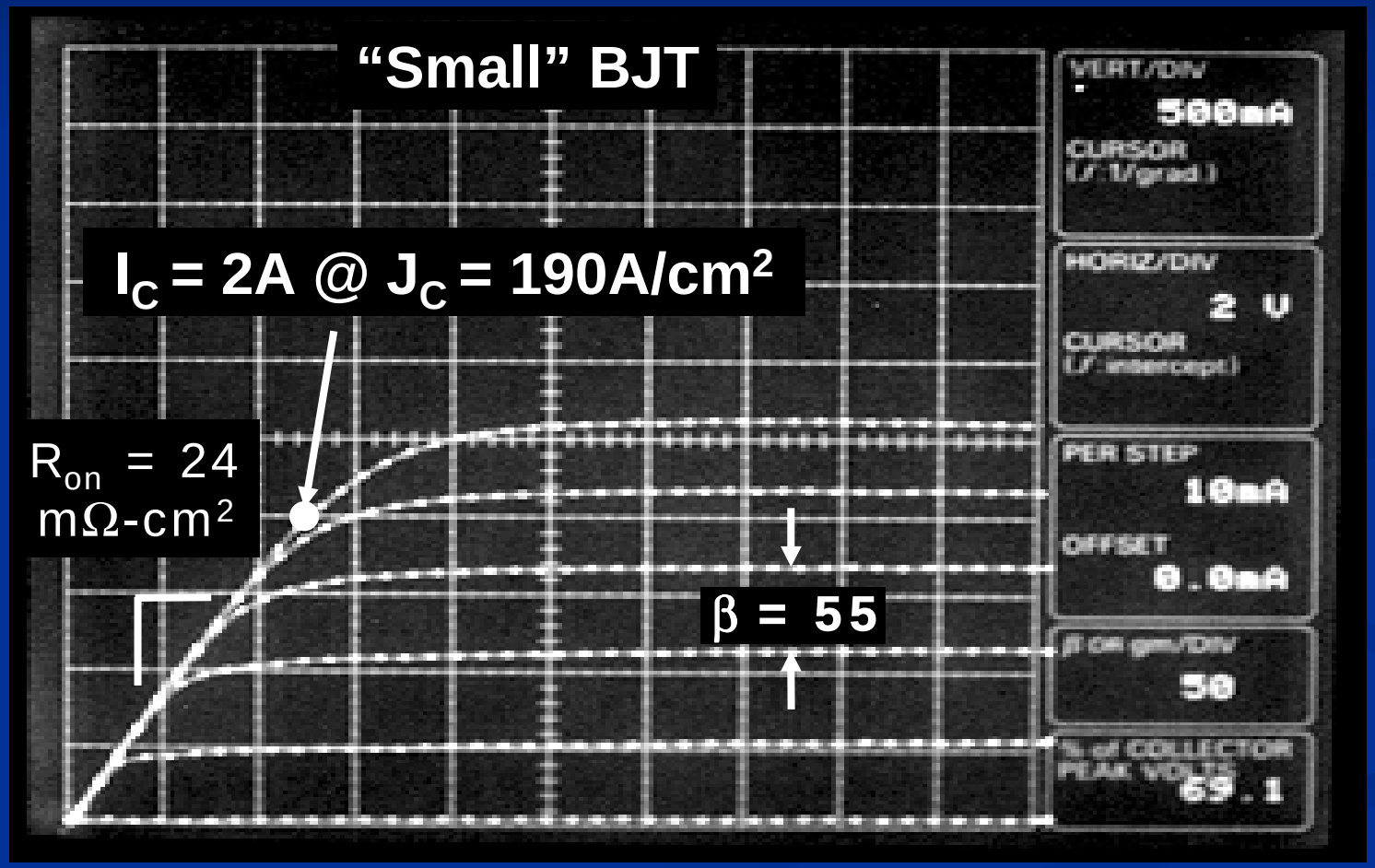
Purdue SiC NPN BJTs

BJT
Active Area
1.5 mm
x 1.4 mm

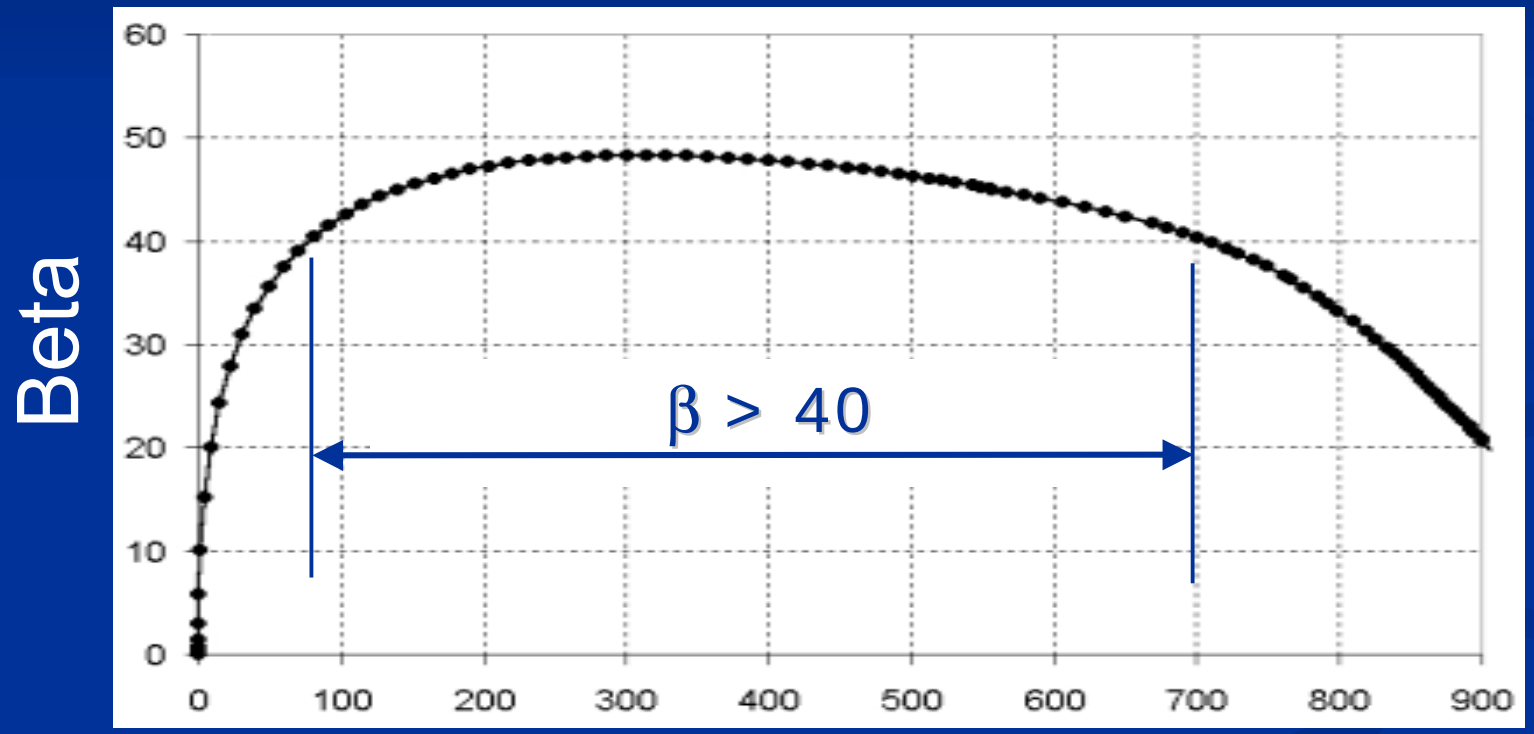


BJT
Active Area
1.5 mm
x 0.7mm

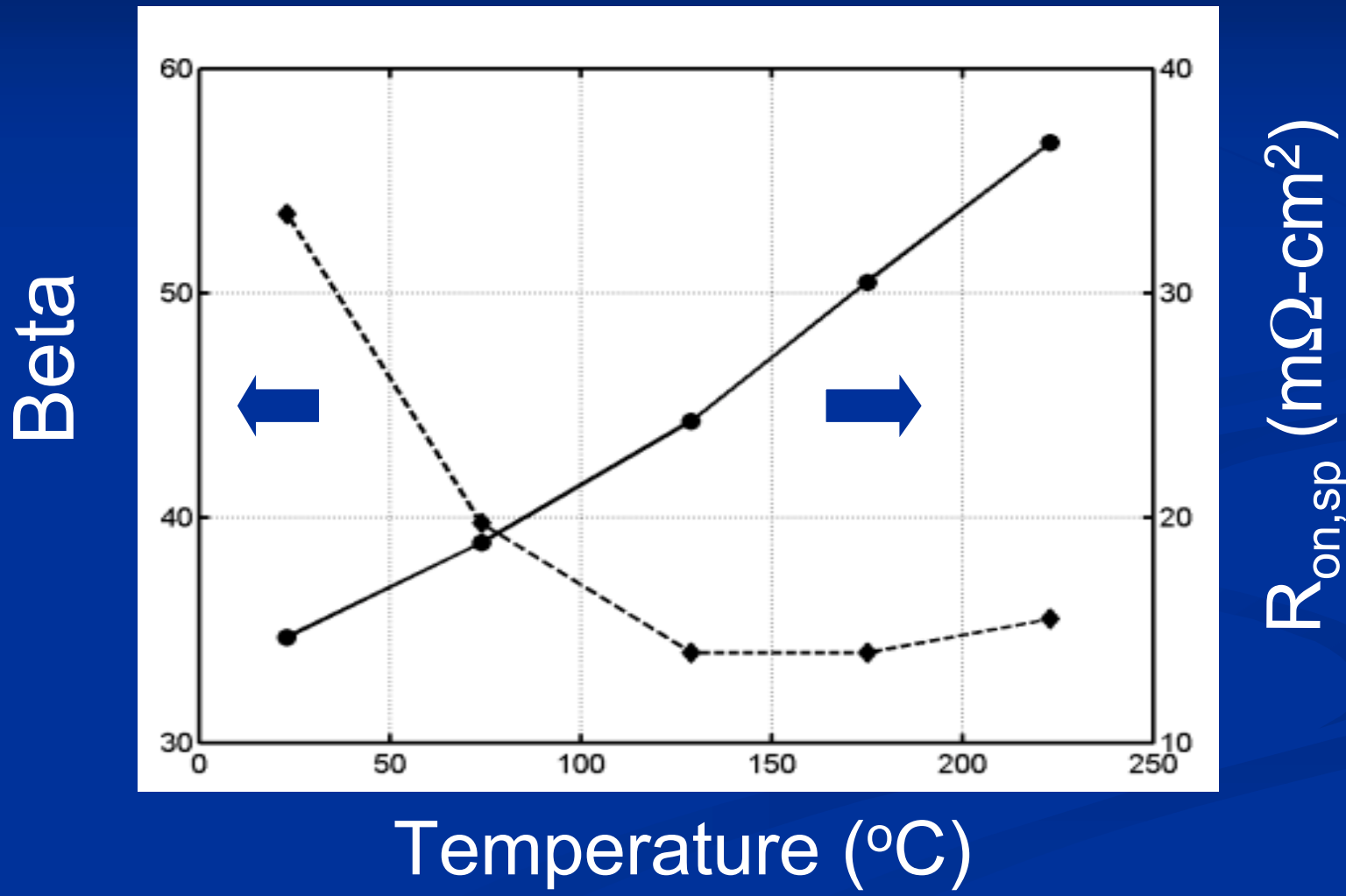
On-State Characteristics



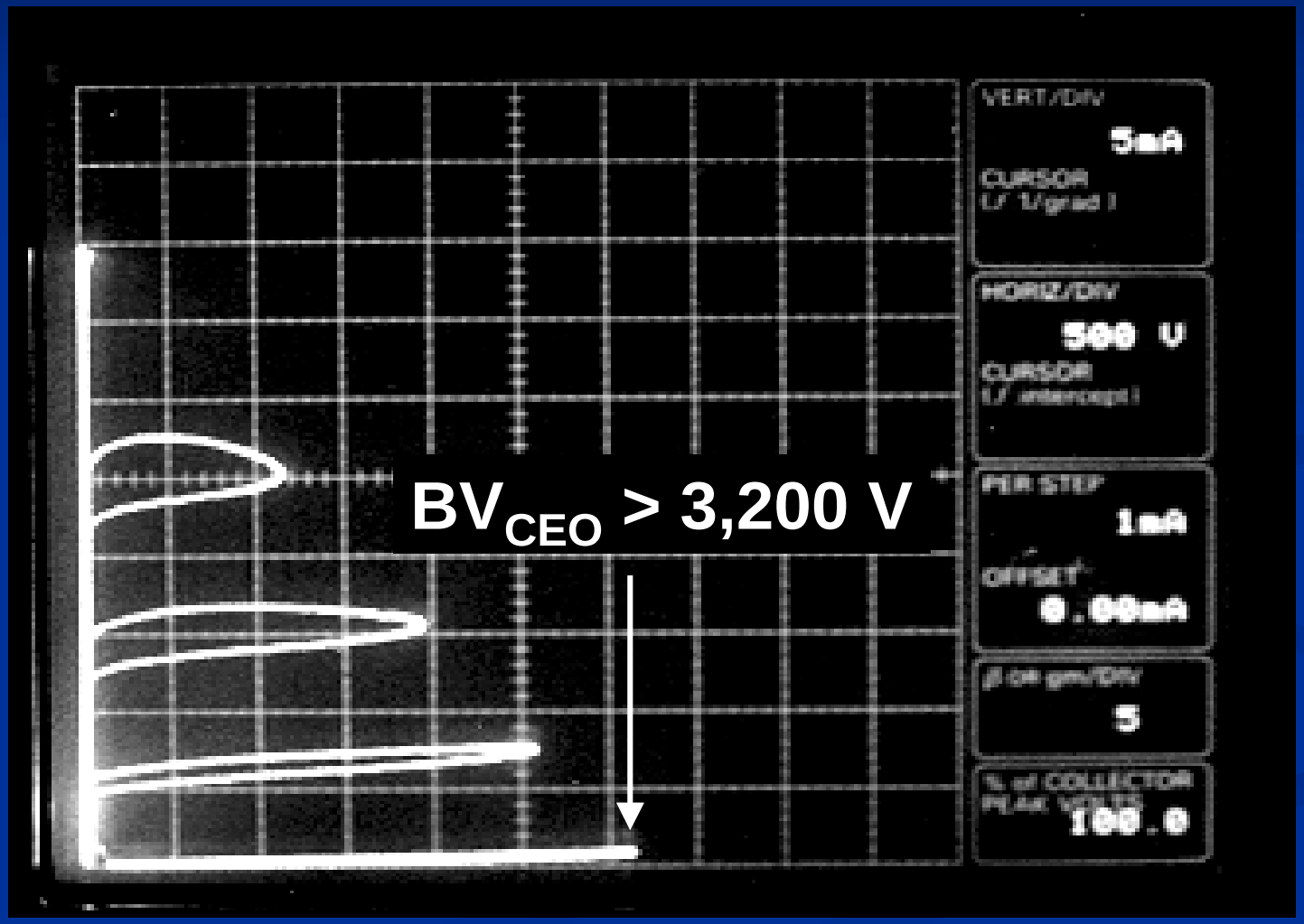
High Current Gain



Temperature Dependence



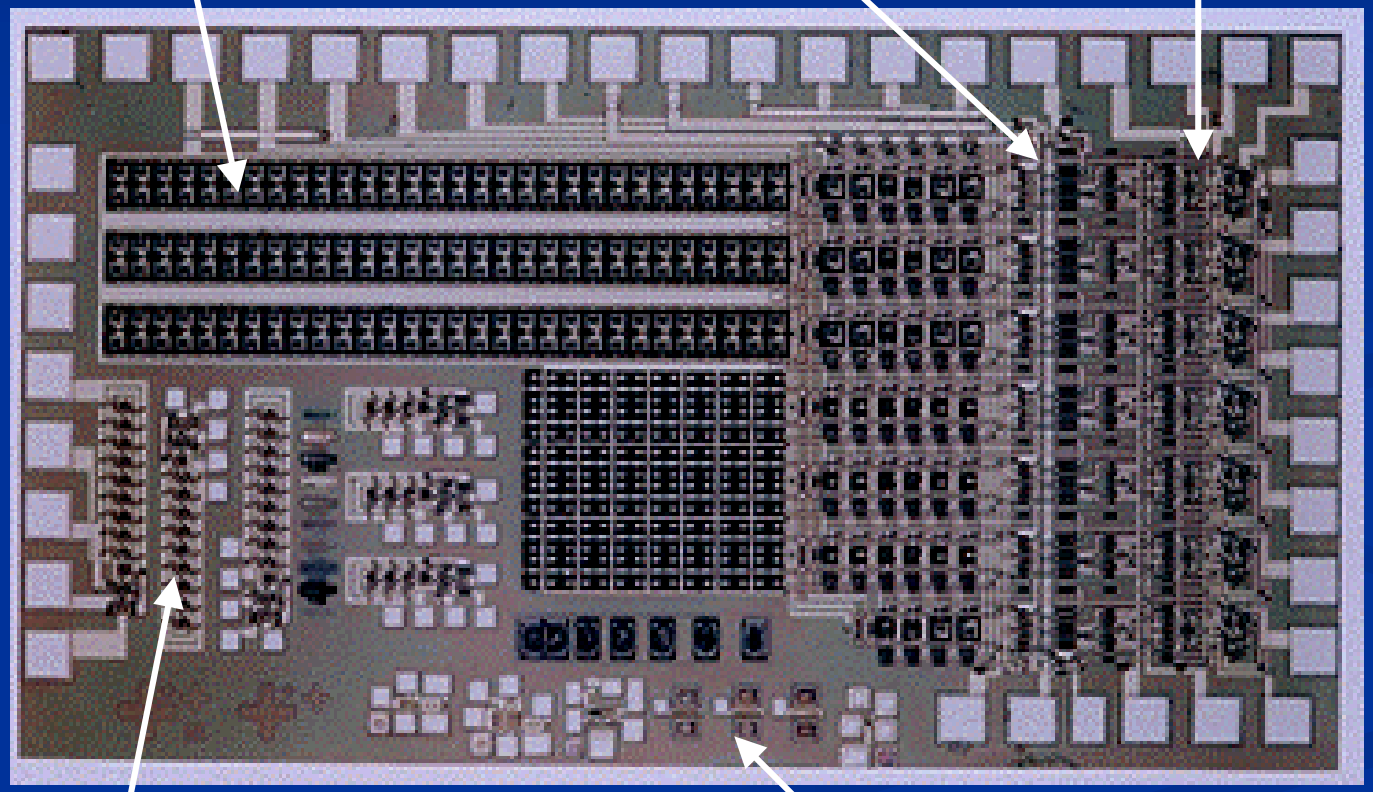
High Blocking Voltage



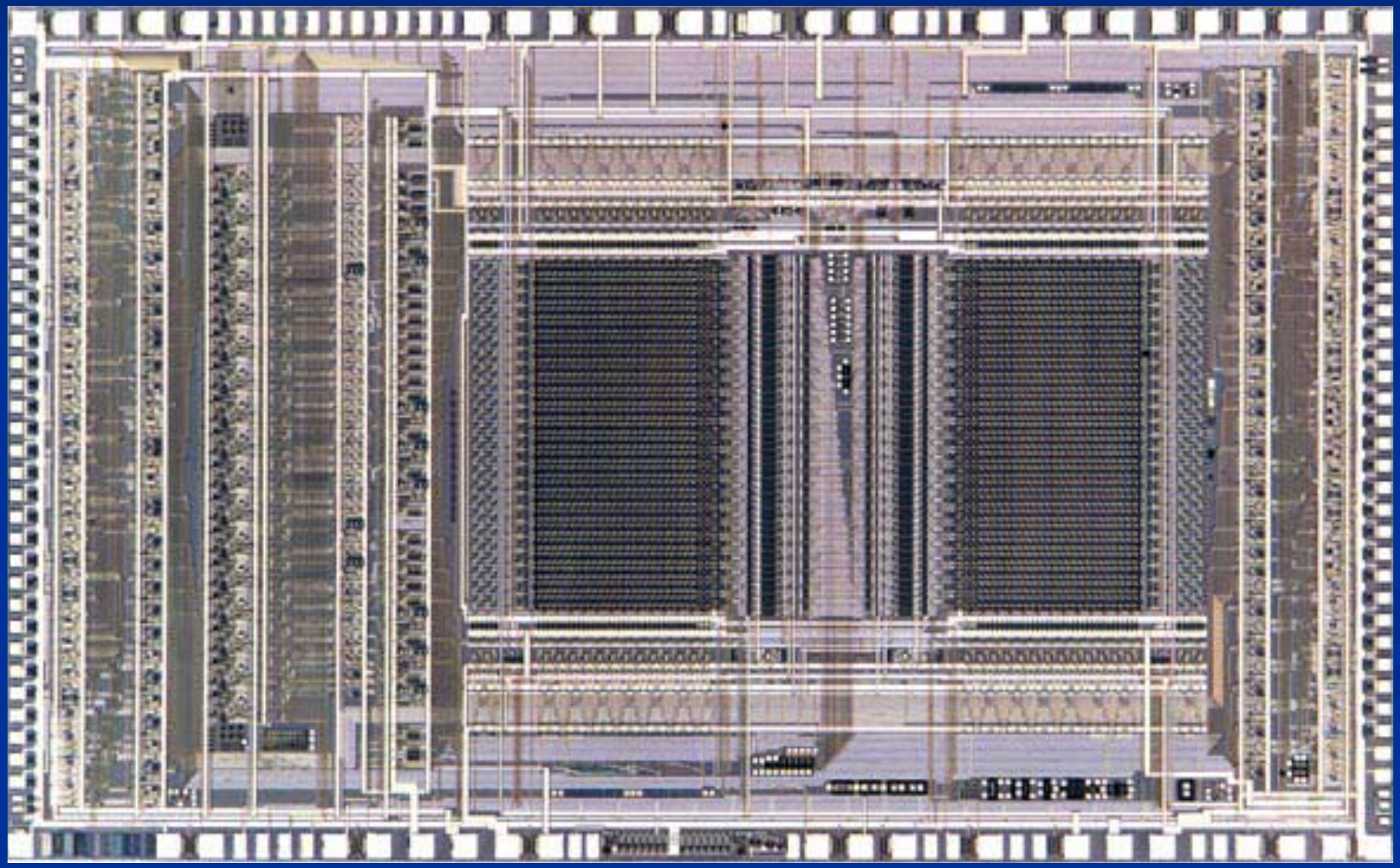
Options for Digital and Linear IC's

- MOS Field Effect Transistors (MOSFETs)
  - *NMOS*
  - *CMOS*
- Bipolar Junction Transistors (BJTs)
- Junction Field Effect Transistors (JFETs)

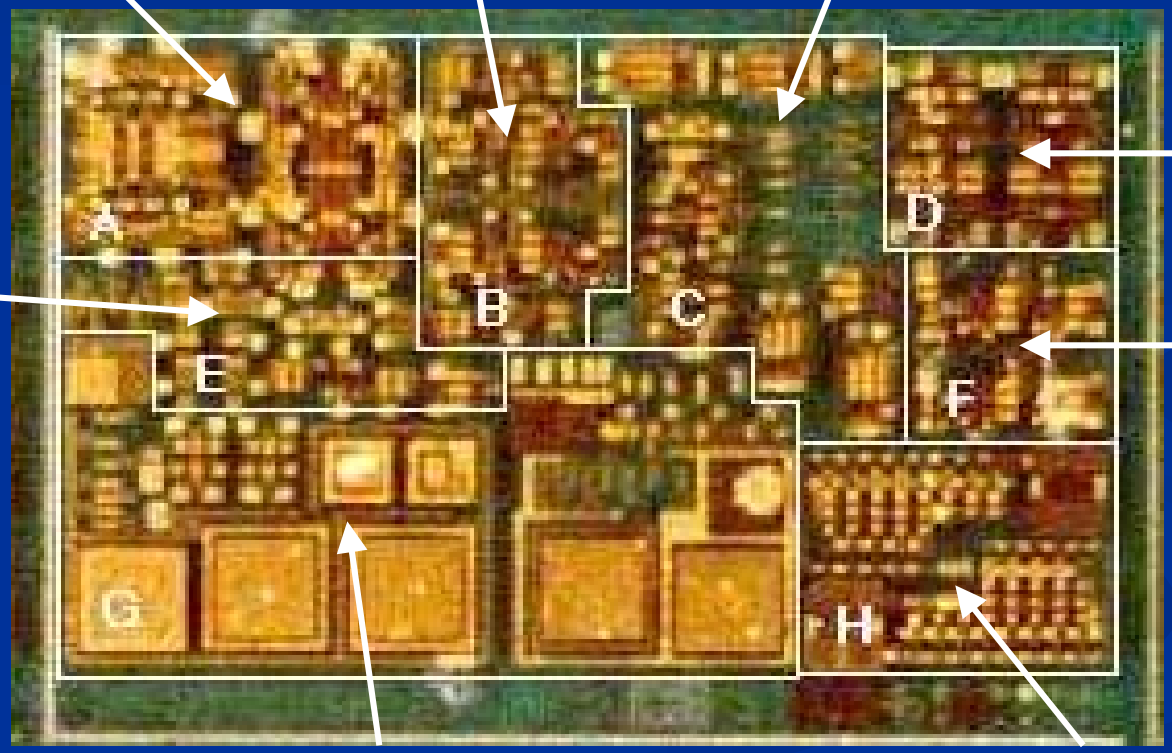
Purdue SiC NMOS IC's (1994)



Cree/Purdue 1 kB SiC BJT NVRAM with NMOS Control Logic (1995)



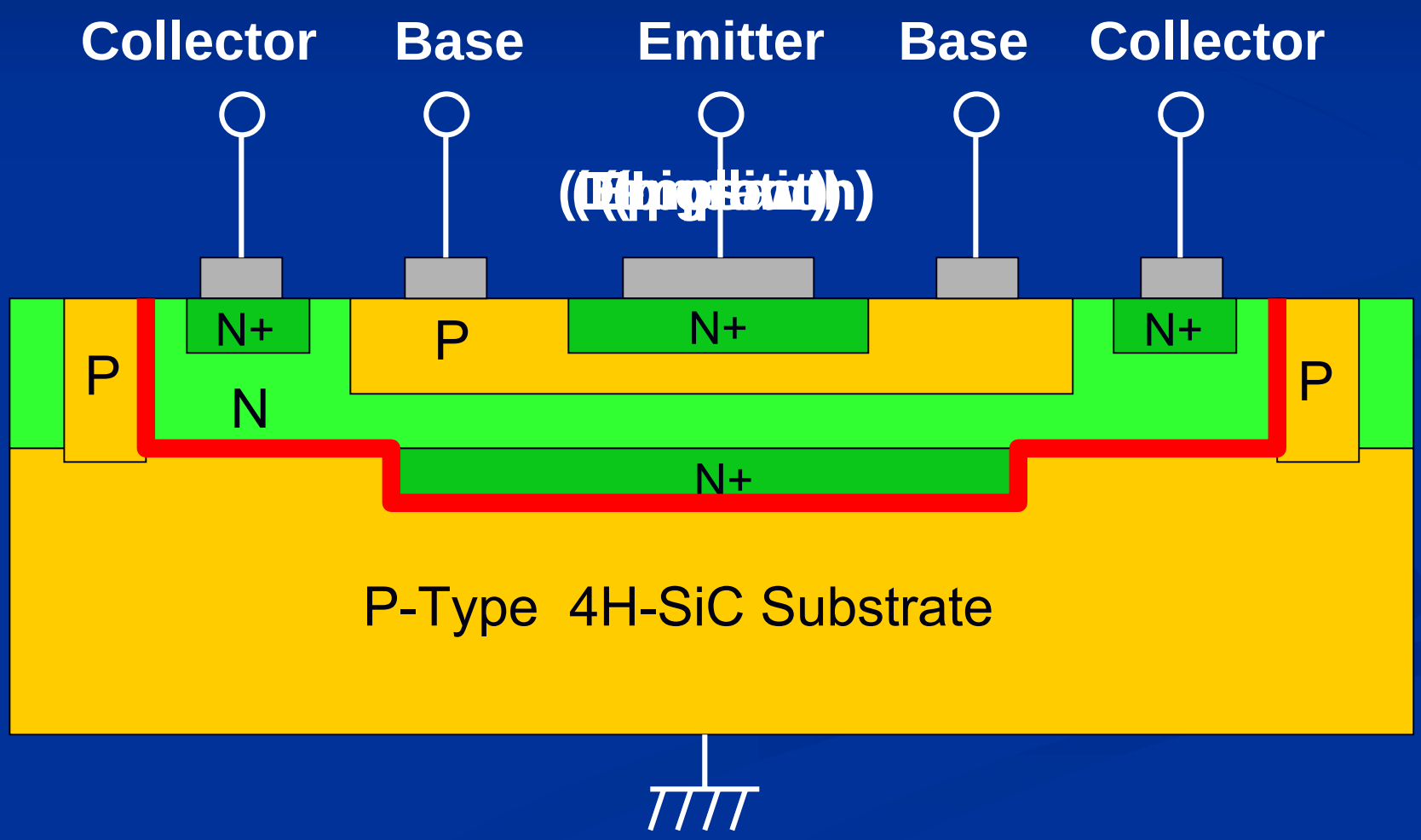
Purdue SiC CMOS IC's (1997)



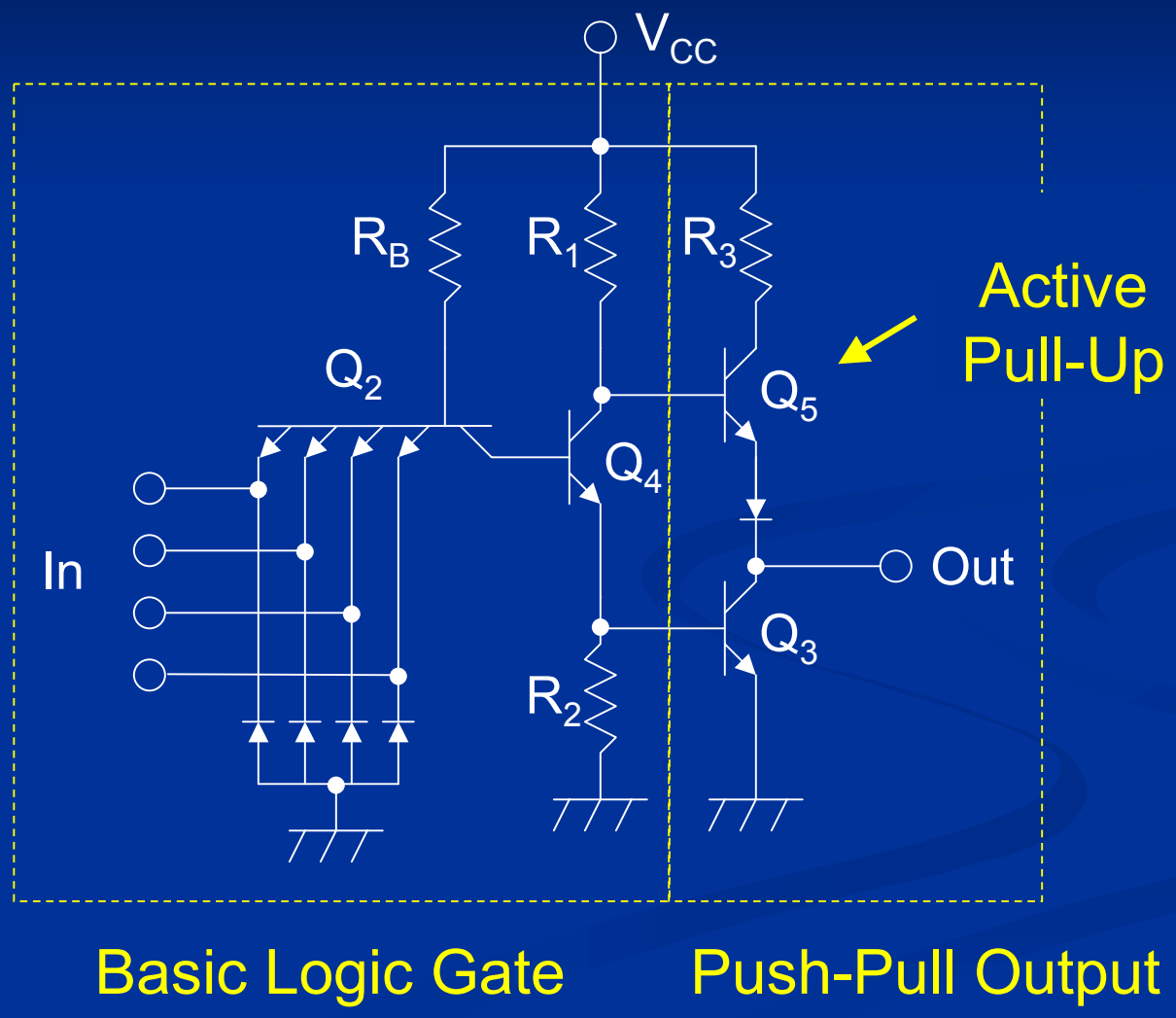
Observations

- SiC MOS IC's are capable of moderately high levels of integration
- SiC MOS IC's are limited to T ≤ 250 °C because of oxide reliability concerns

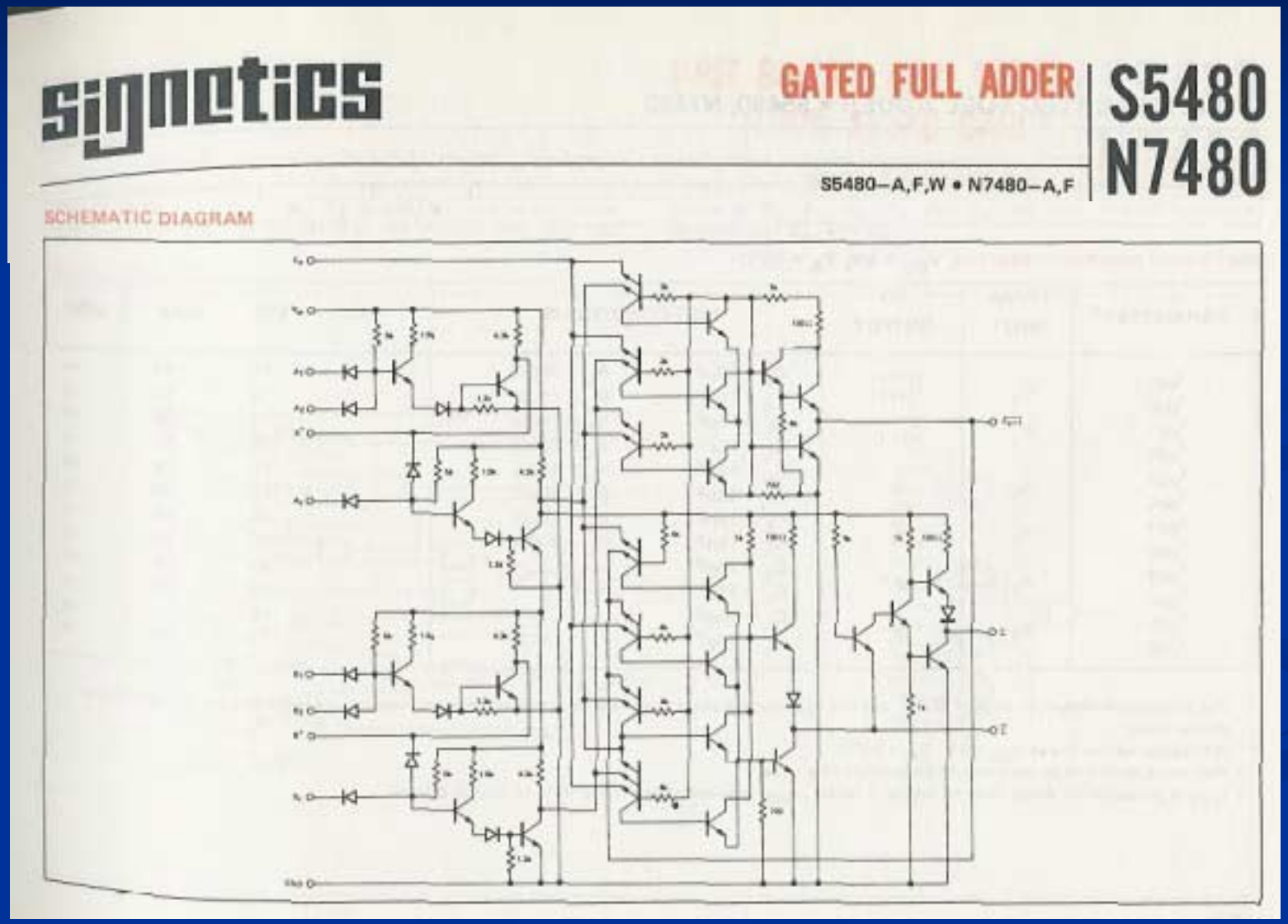
SiC Bipolar IC's



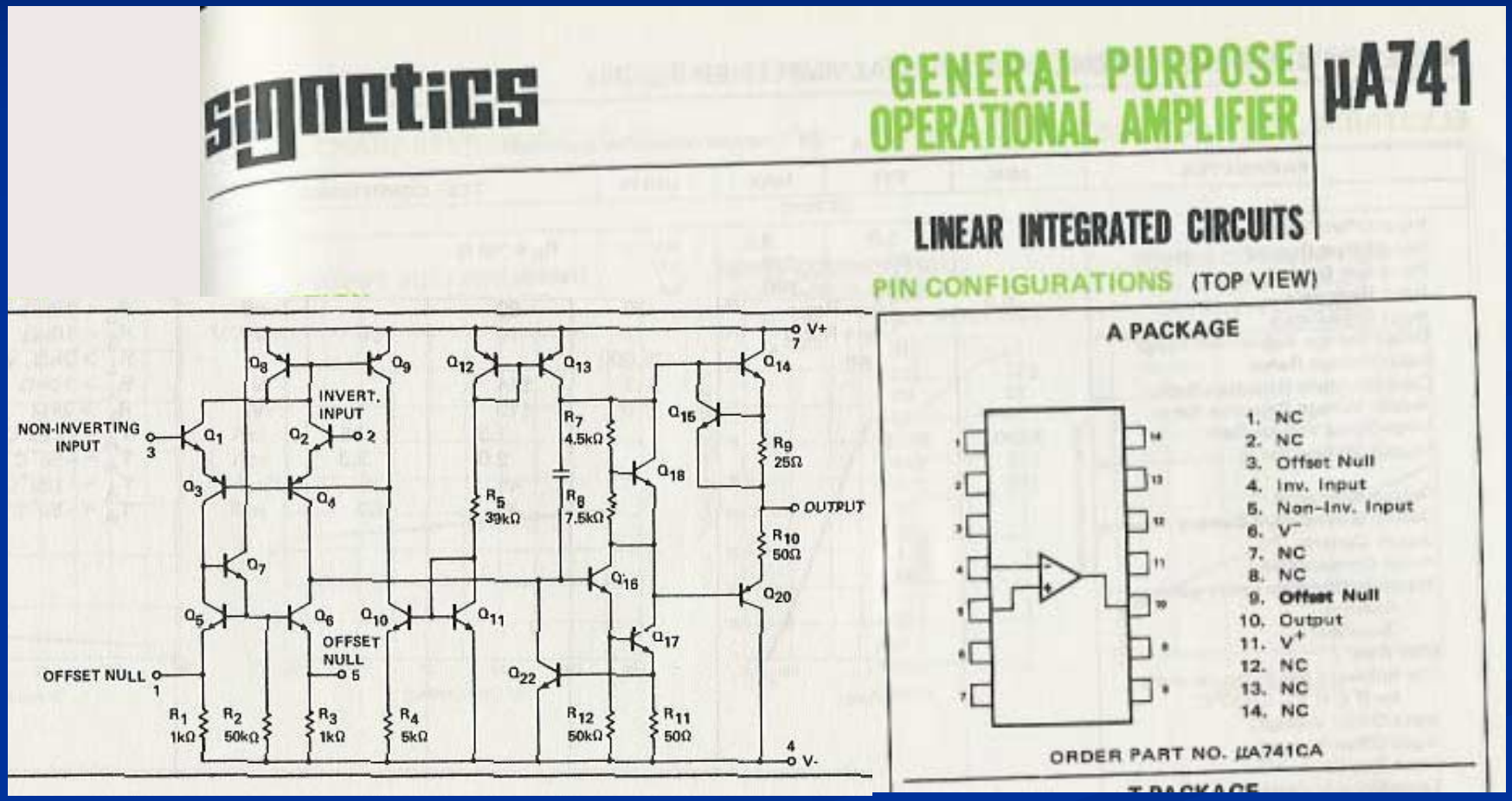
TTL 4-Input NAND Gate



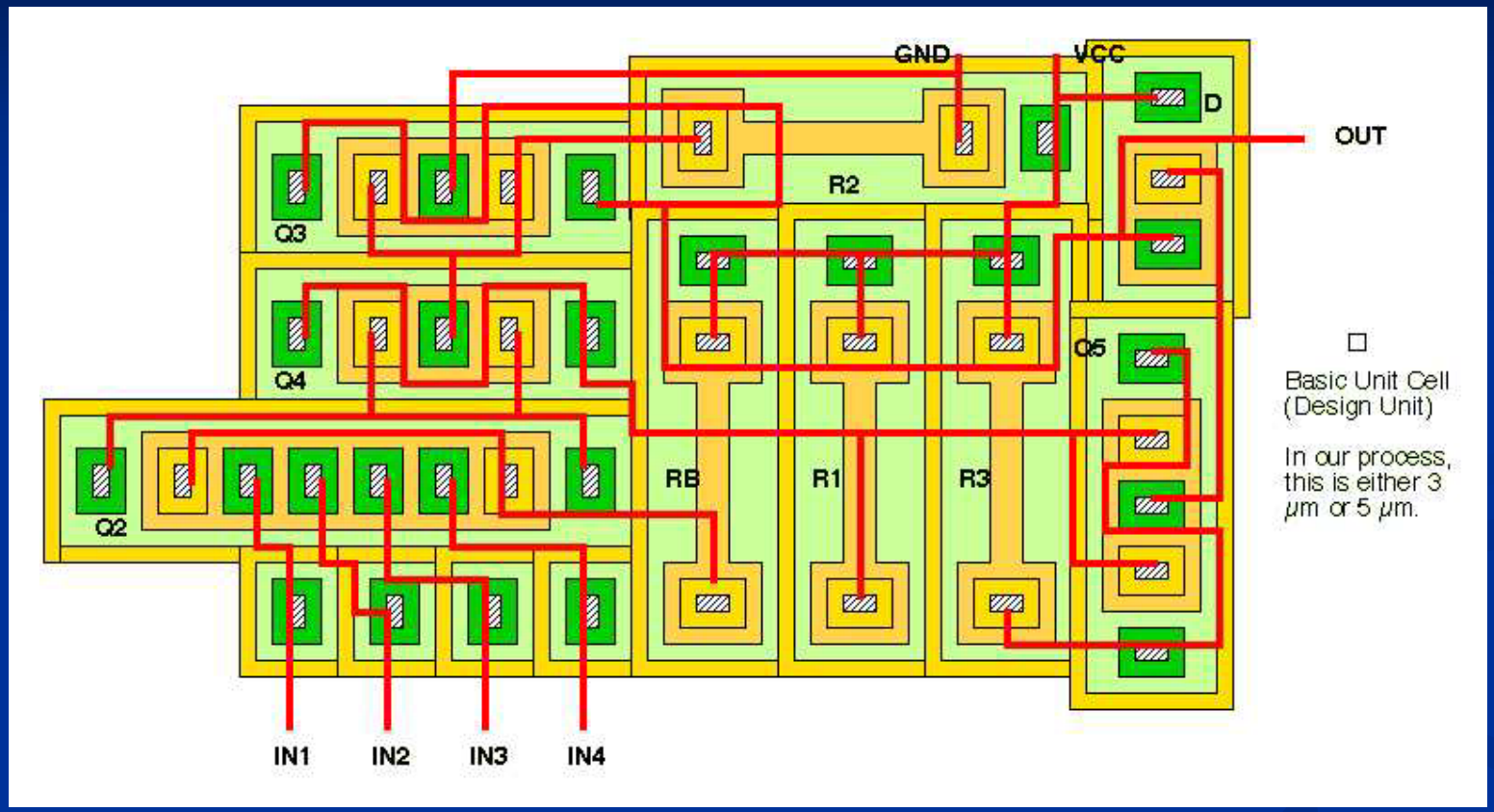
TTL Logic Family



BJT Linear ICs

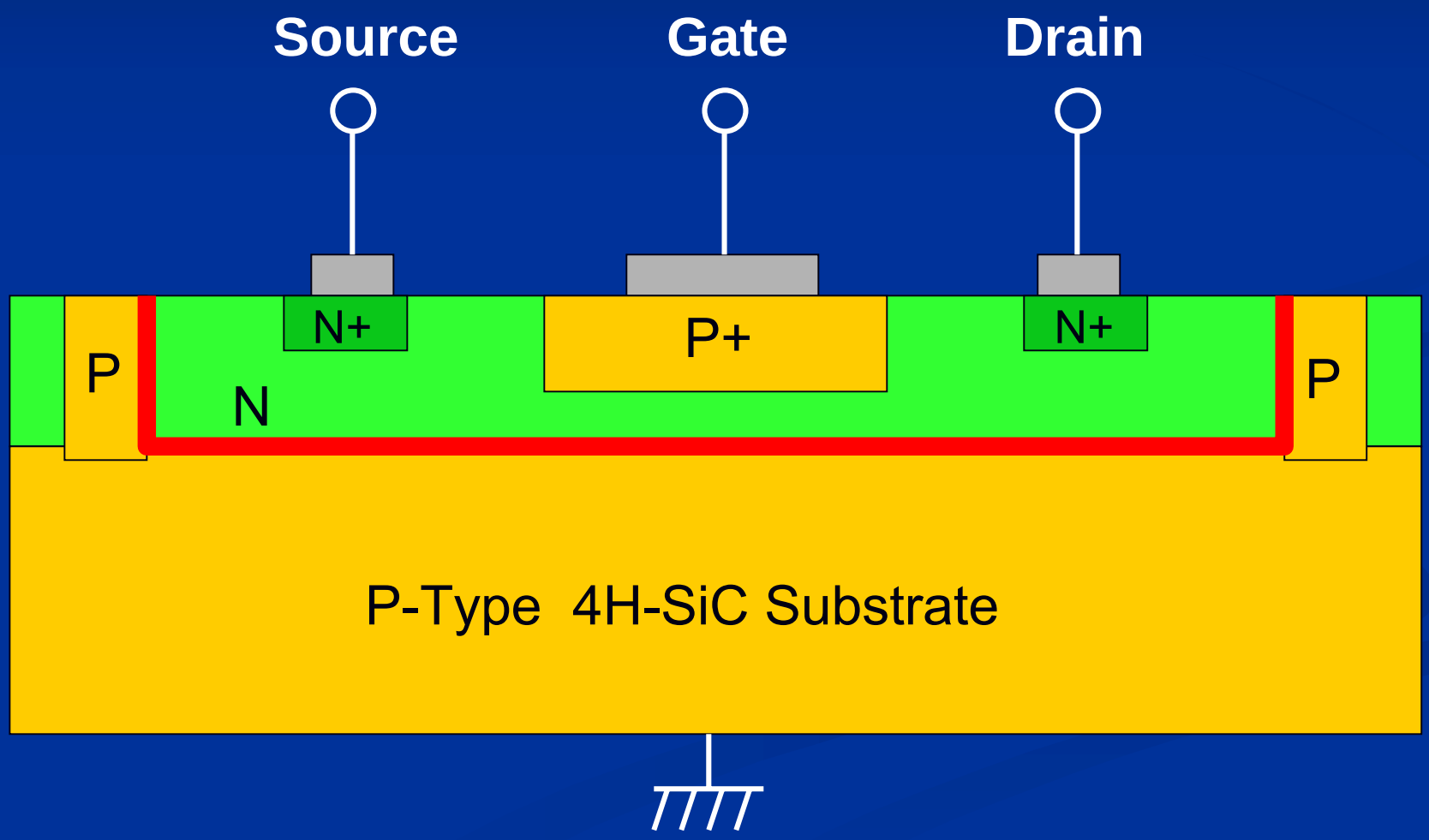


Layout of TTL 4-NAND Gate

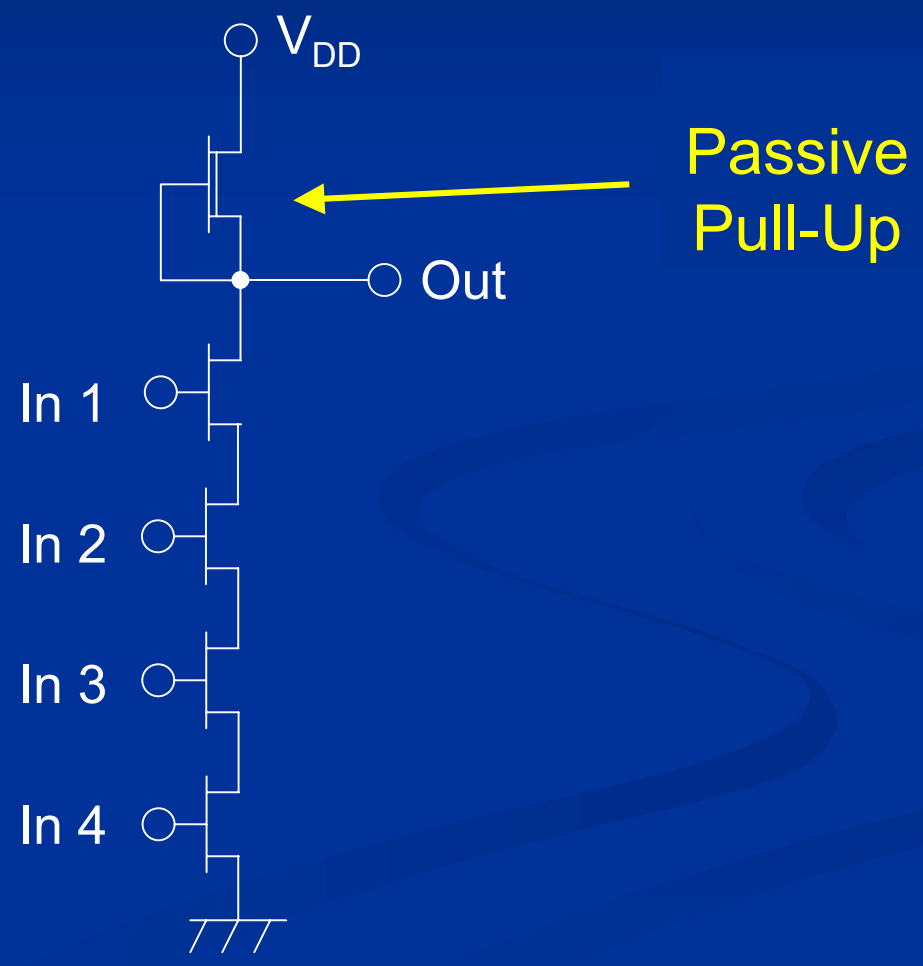


Area = 2.2×10^{-4} cm^2. A 2x2 mm^2 chip would contain 182 TTL gates.

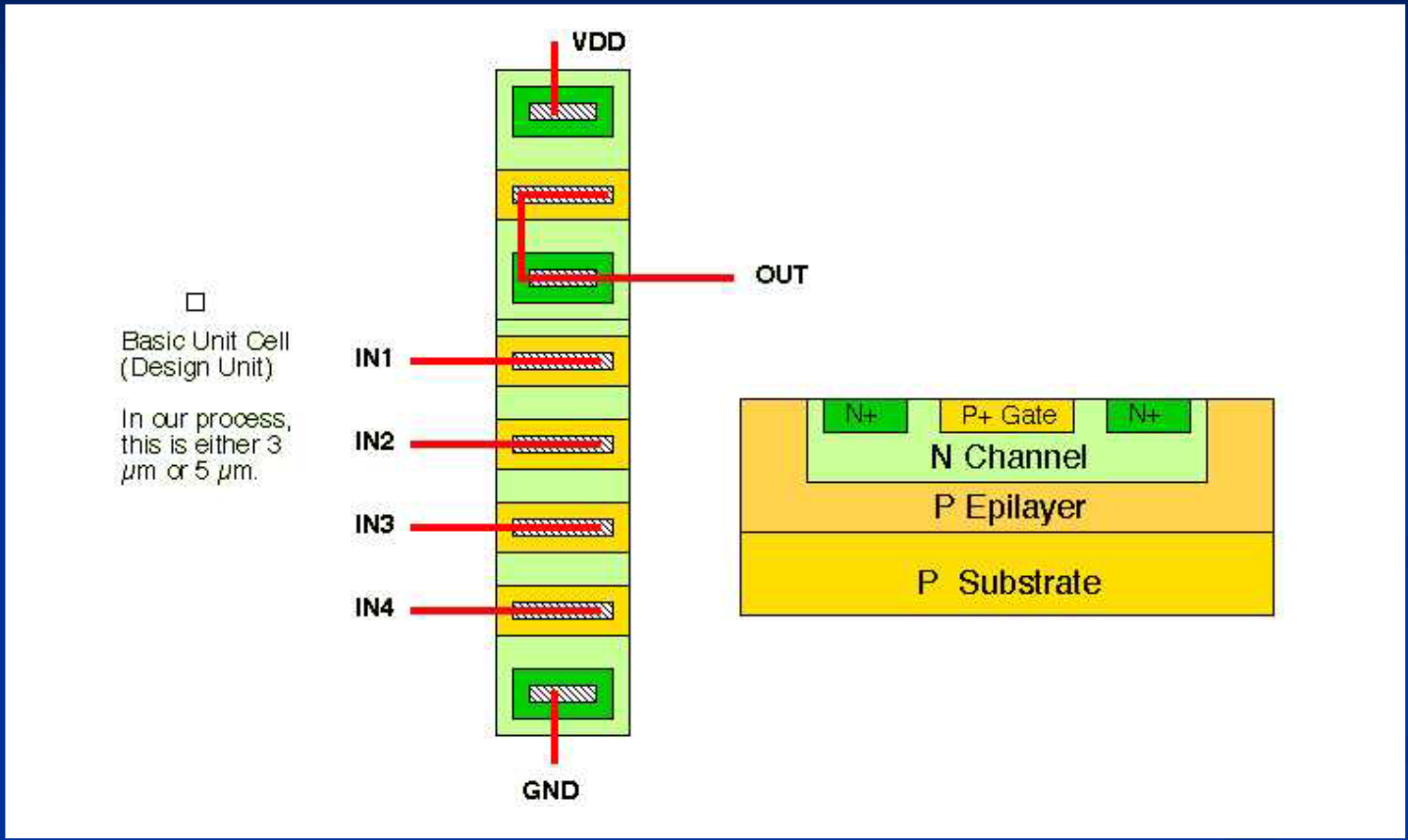
SiC JFET IC's



Direct-Coupled FET Logic (DCFL) JFET 4-NAND Gate



Layout of JFET 4-NAND Gate

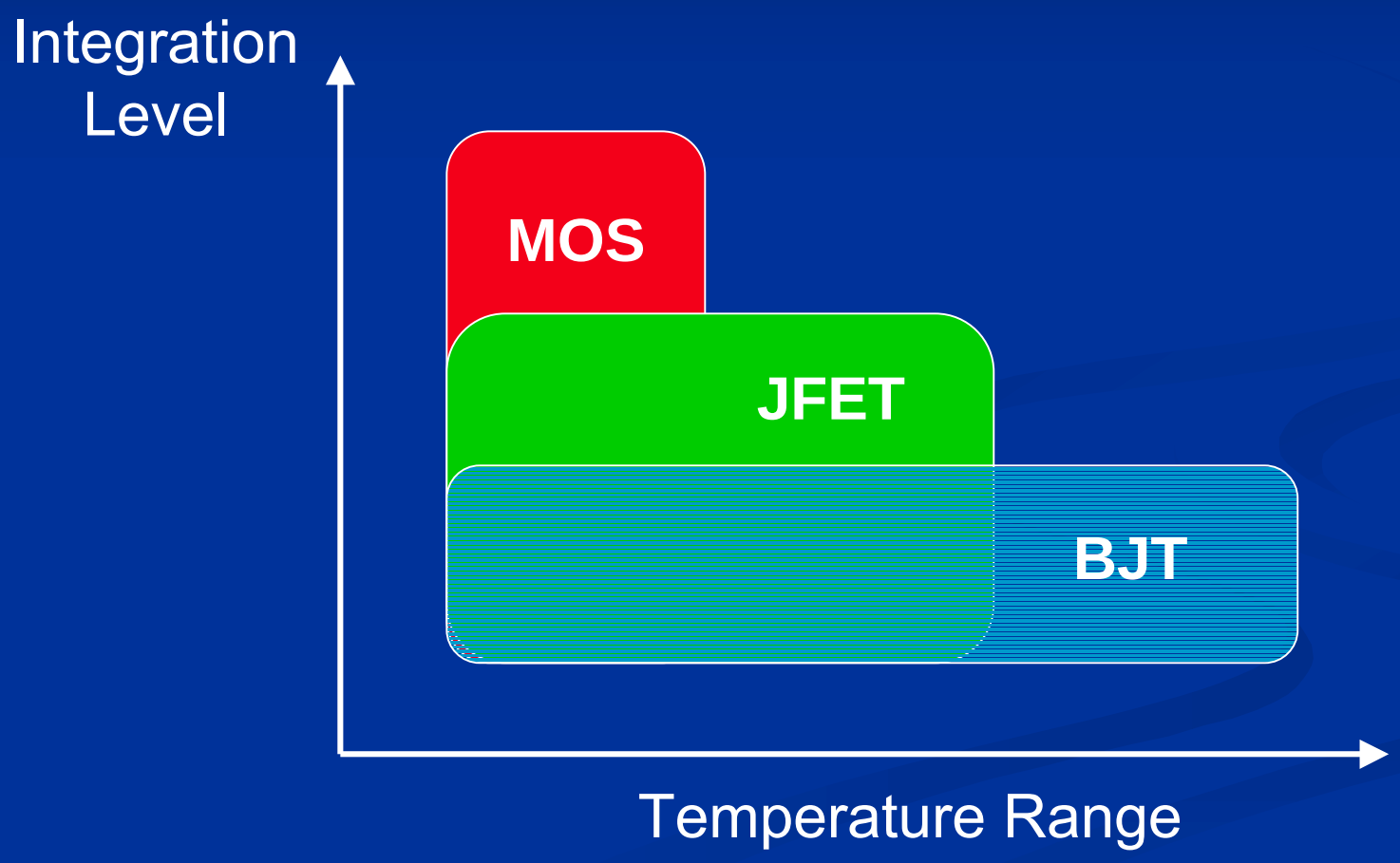


Area = 3.0×10^{-5} cm^2. A 2x2 mm^2 chip would contain 1355 JFET gates.

Observations

- JFET gates are smaller than BJT gates.
- TTL gates incorporate a push-pull output with active pull-up. This reduces the temperature sensitivity of TTL gates.
- Because of their passive pull-up, JFET gates are more sensitive to temperature.

Comparison of Technologies



Other Applications

- Microwave Components

  (both transmit and receive)

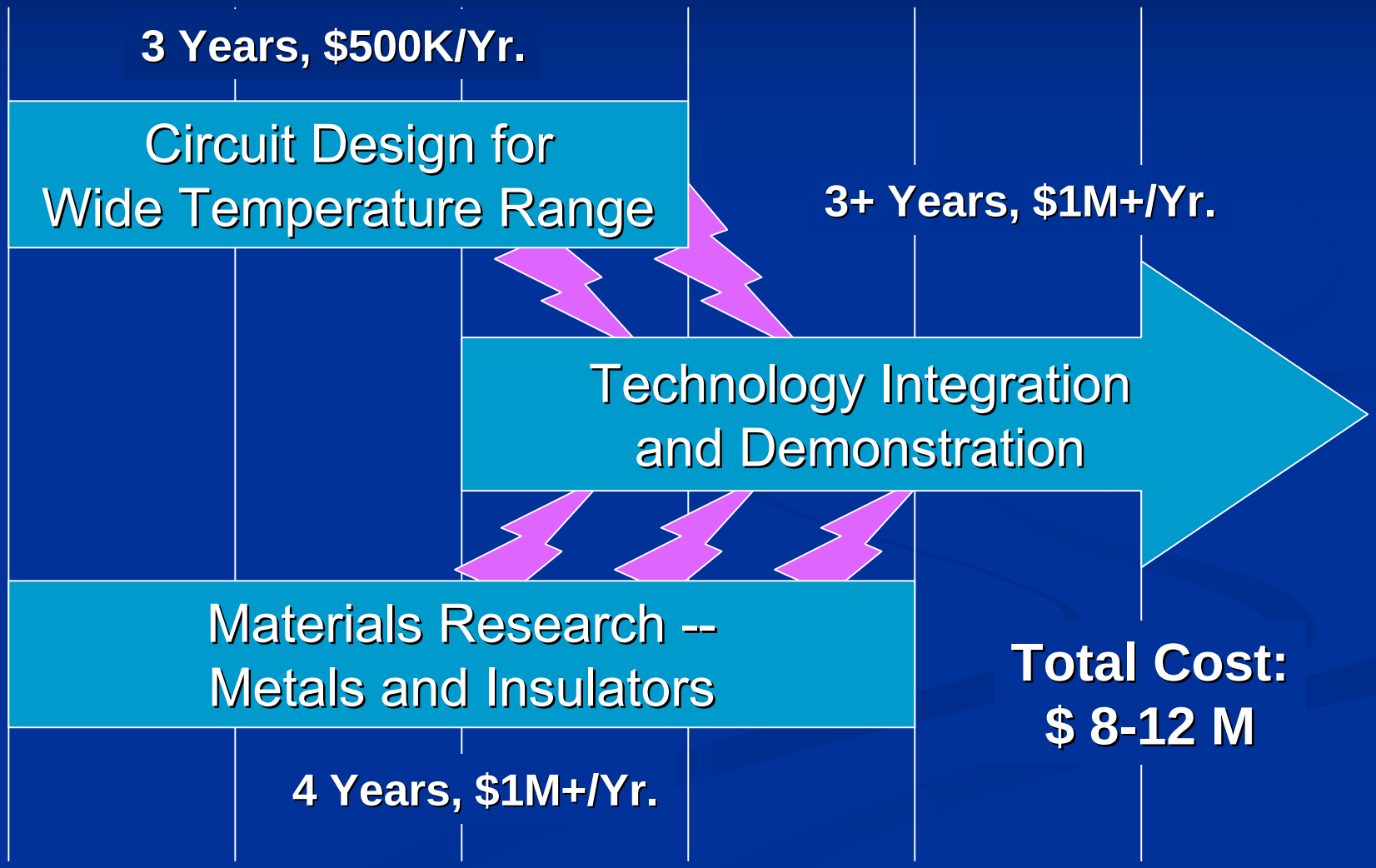
- Rugged Sensors

  (gas sensors, optical sensors, CCDs...)

Challenges

- Design Challenges
  - *Assuring proper circuit operation over a wide temperature range (0 to >400 °C)*
- Materials Challenges
  - *Control of critical device parameters*
  - *Assuring high temperature reliability of...*
    - *Passivation layers*
    - *Ohmic contact metalurgy*
    - *Interconnect metalurgy*
  - *Assuring desired level of radiation tolerance*

Suggested Development Program



Total Cost:
$ 8-12 M

Summary

- SiC electronics are ideally suited for extreme environments (high temperature and radiation)
- MOSFETs will be limited to $T \leq 250$ °C, while BJTs and JFETs can operate at $T \geq 400$ °C
- Substantial progress can be made by a five-year development program costing $8-12M

For more information...

www.ecn.purdue.edu/WBG