Precision Data Conversion in High-Temperature Systems

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Presentation Summary

- High-Temperature Electronics Design Challenges
- Candidate ADC Topologies
- $\Sigma\Delta$ ADC Overview
- Integrated Circuit Fabrication Processes & Temperature Limitations
- SOS $\Sigma\Delta$ Modulator Examples
- Conclusion
- Ongoing Research Areas

Precision Analog Design For High Temperature Applications Is Very Challenging

- Device Degradation With Increasing Temperature
  - Threshold voltage (V_t) shift
  - Mobility reduction (g_m degradation)
  - Increased parasitic leakages
  - Increased device noise
- Increased Power Consumption
- Reliability Issues
  - Metal Electromigration
  - Packaging

Comparison of Si-Based Fabrication Processes For High-Temperature Application

Bulk CMOS

- T 200°C
- Mature
- Many Foundries
- Inexpensive

Silicon Carbide (Si-C)

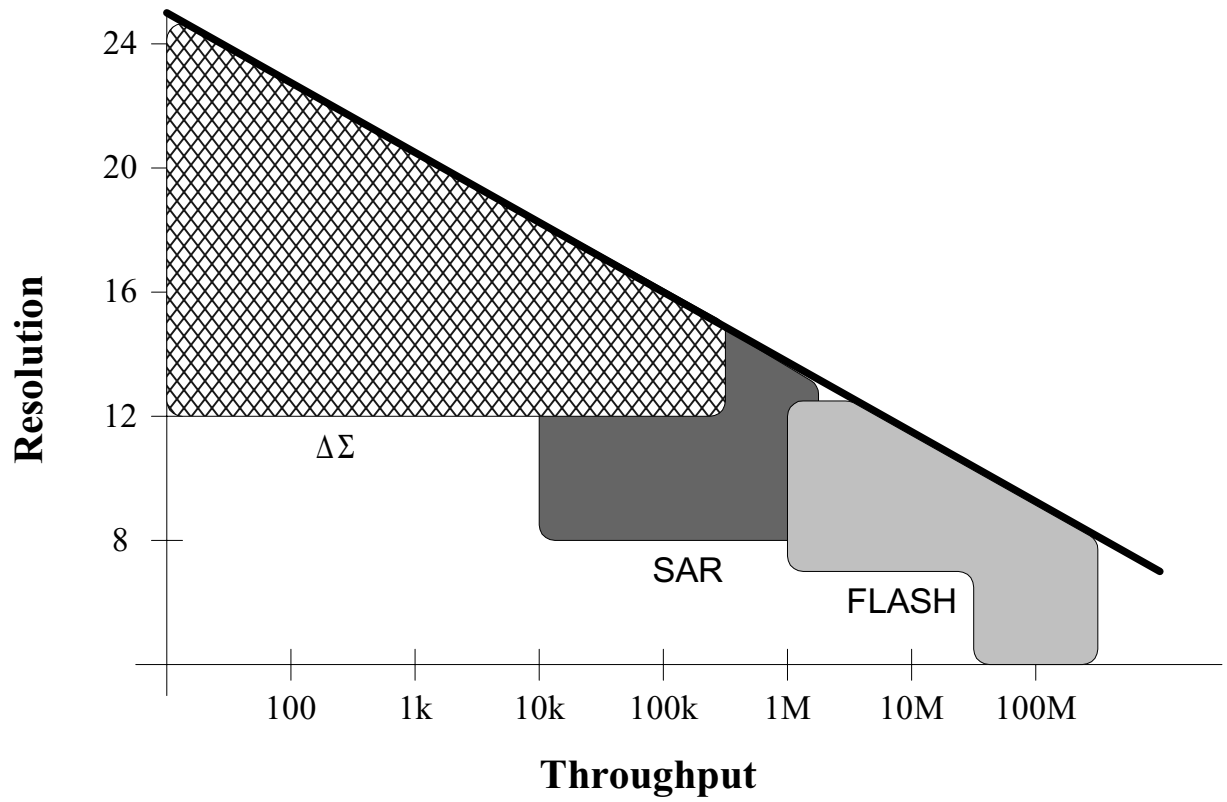
- T 600°C
- Maturing
- Very Limited Availability
- Very High Cost

Silicon-on-Insulator (SOI) – Silicon-on-Sapphire (SOS)

- T 350°C (500 °C reported)
- Fairly Mature
- Available
- Moderate Cost

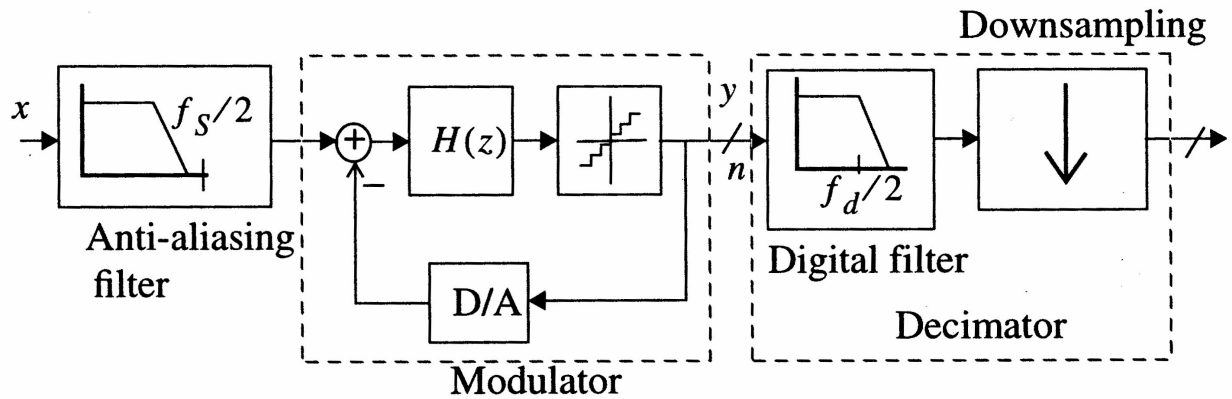
SOI/SOS Technologies Provide a Mature, Commercially Available Technology With Acceptable Temperature Performance

ADC Topology Overview – Speed & Resolution Tradeoff



Nyquist Rate Converters Are Limited to ~15 bits

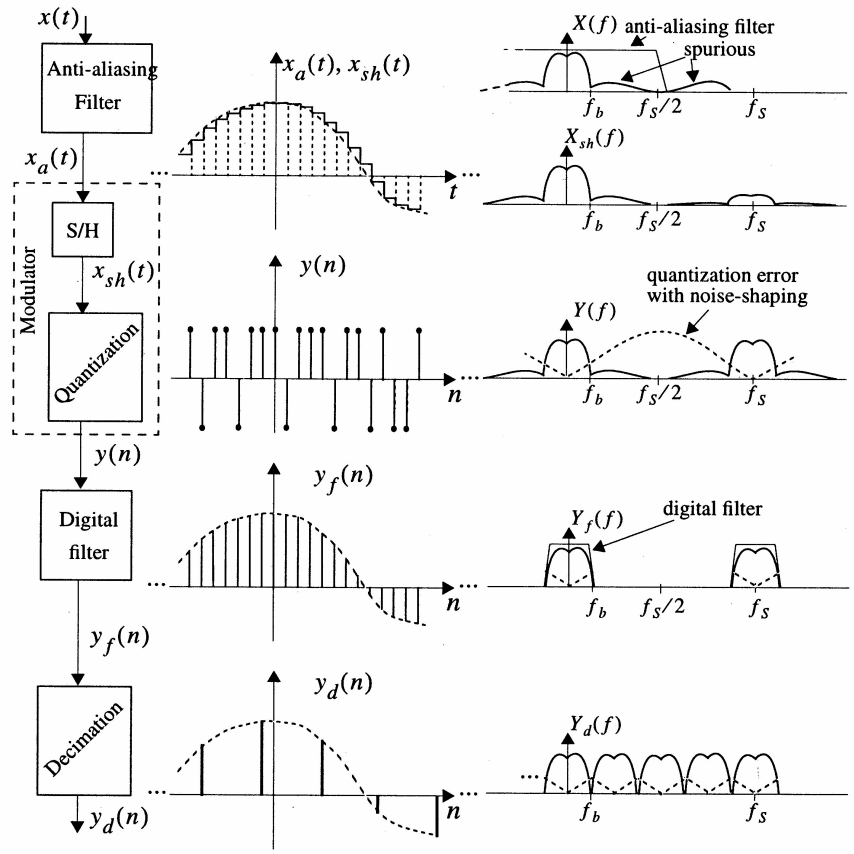
ΣΔ ADCs Employ Oversampling, Noise Shaping, and Digital Filtering to Produce High-Resolution Results



- Input Signal is Heavily Oversampled
- Quantization Noise is Shaped to Suppress the Noise Component in the Input Signal Bandwidth
- Digital Filter Recovers the In-Band Signal and Down-Samples to the Nyquist Rate

A Low-Speed, High-Resolution Output Is Obtained Using A High-Speed, Low-Resolution Sampler

ΣΔ Converters - Oversampling & Noise Shaping Advantages



High-Resolution Results Are Obtained Using Low-Resolution Circuit Blocks

Literature Review (1988-present)

- **~1800 ΣΔ-related papers in bulk-CMOS**
- **Only 6 papers reporting ΣΔ modulators in SOS or SOI**
  - 1st-2nd and 4th order modulators reported
  - Up to 15-bit resolution
  - Temperatures up to 350ºC (with degraded resolution)

Published SOS/SOI Modulators (1988-present)

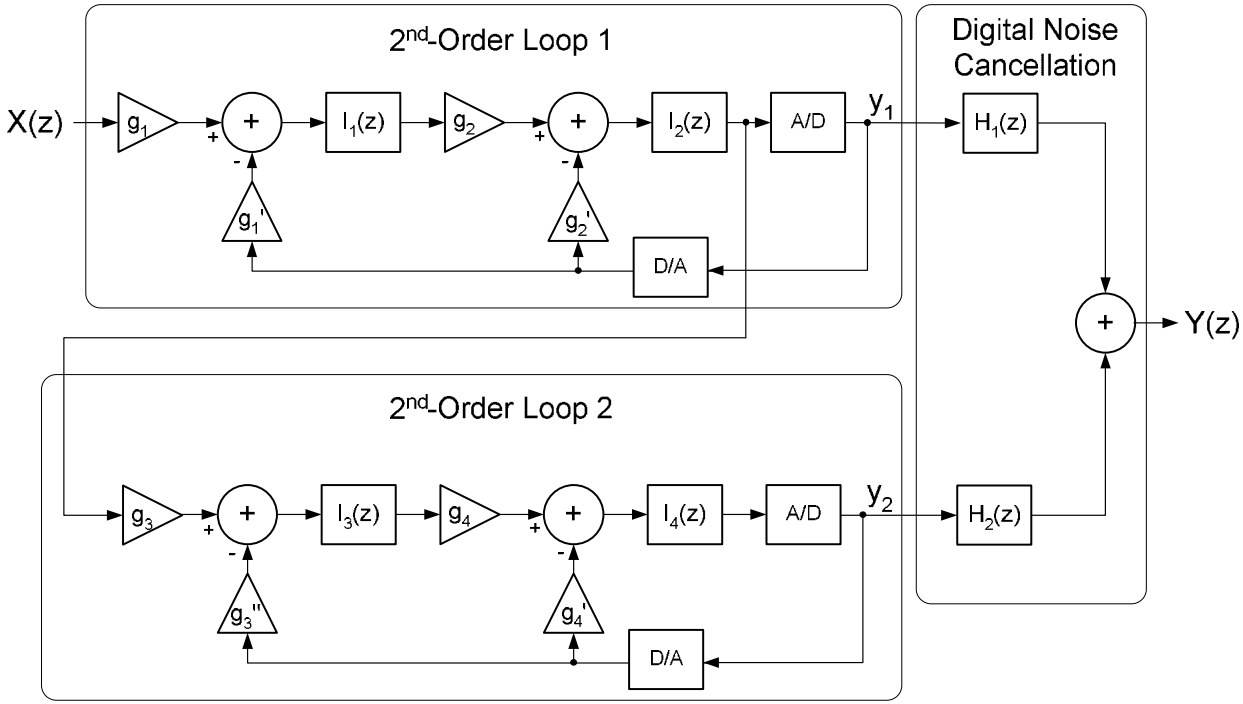
Reference	T (C)	Resolution (bits)	DOR (S/s)	Power (mW)	Process / Supply	Architecture	OSR	Internal Resolution
Viviani96	27	9.3*	781	0.06	3μm SOI-CMOS / 2V	1st order	128	1-bit
	350	4.7*	3906	0.5	3μm SOI-CMOS / 2V	1st order	128	1-bit
Viviani99	30	11	15625	---	SOI-CMOS / 5V	2nd order	64	1-bit
	250	10	15625	---	SOI-CMOS / 5V	2nd order	64	1-bit
	300	9	15625	---	SOI-CMOS / 5V	2nd order	64	1-bit
Swaminathan99	27	8*	400000	0.3	0.25μm SOI-CMOS / 1V	2nd order	125	1-bit
Edwards99	27	9.7	126000	---	1.5μm SOS-CMOS / 5V	1st order	128	4-bit
Ericson02	27	15.4	2000	25	0.5μm SOS-CMOS / 3.3V	2nd/4th order	256	1-bit
	150	14.7	2000	25	0.5μm SOS-CMOS / 3.3V	2nd/4th order	256	1-bit
	200	13.4	2000	27	0.5μm SOS-CMOS / 3.3V	2nd/4th order	256	1-bit

ΣΔ Modulator Design Example

2nd- and 4th-Order ΣΔ Modulators Fabricated in 3.3V 0.5μm SOS-CMOS for High-Temperature Applications

(Proceedings of the 2002 IEEE International SOI Conference, Williamsburg, VA, Oct. 2002.)

Selection of the Modulator Architecture was Performed to Optimize High Temperature Operation



- 4th-order noise shaping (L=4)
- Oversampling ratio = 256 (M=256)
- Single-bit internal quantization (N=1)
- f_s = 512kHz

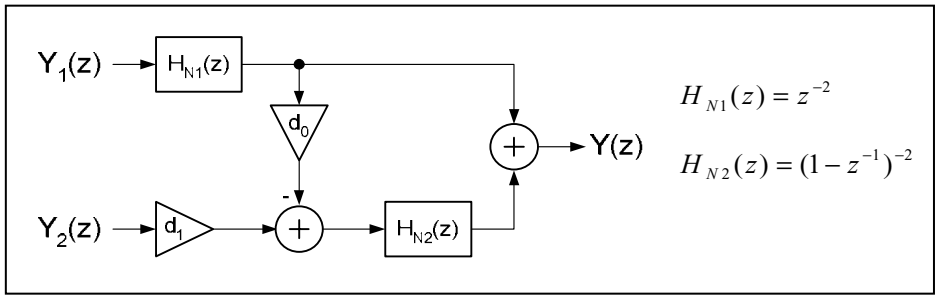
Ideal Transfer Function

$$Y(z) = z^{-4}X(z) + (1 - z^{-1})^4 E_{Q2}(z)$$

- Cascaded architecture is conditionally stable
- Gain settings selected to maximize tolerance of capacitor mismatch

Digital Noise Cancellation

$$Y(z) = Y_1(z)H_1(z) + Y_2(z)H_2(z)$$



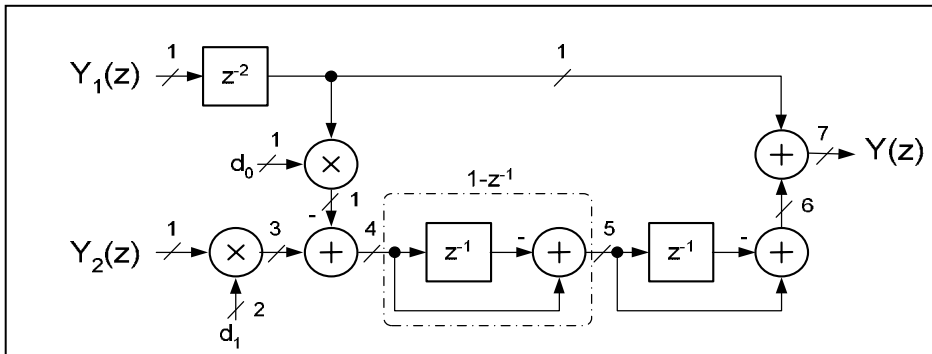
$$H_{N1}(z) = z^{-2}$$

$$H_{N2}(z) = (1 - z^{-1})^{-2}$$

$$Y_1(z) = \frac{\left(\frac{g_1}{g_1'}\right) z^{-2} X(z) + (1 - z^{-1})^2 E_{Q1}(z)}{1 + z^{-1}\left(\frac{g_2'}{g_1' g_2} - 2\right) + z^{-2}\left(2 - \frac{g_2'}{g_1' g_2}\right)}$$

$$Y_2(z) = \frac{\left(\frac{1}{g_3''}\right) z^{-2} X_2(z) + (1 - z^{-1})^2 E_{Q2}(z)}{1 + z^{-1}\left(\frac{g_4'}{g_3'' g_4} - 2\right) + z^{-2}\left(2 - \frac{g_4'}{g_3'' g_4}\right)}$$

$$X_2(z) = Y_1(z)(g_3 - g_3') - g_3 E_{Q1}(z)$$



$$Y(z) = z^{-4} X(z) + \beta (1 - z^{-1})^4 E_{Q1}(z)$$

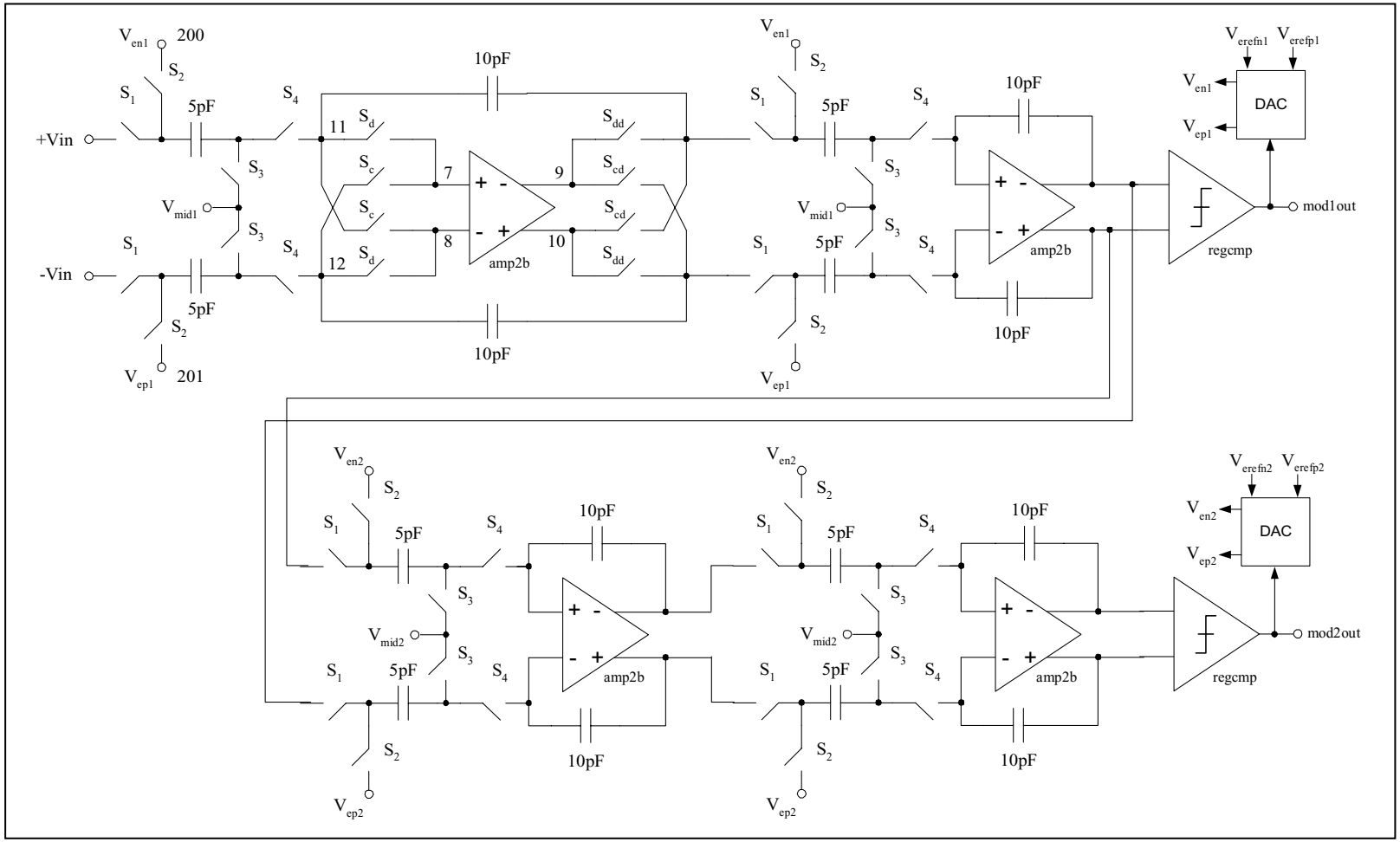
$$\beta = \frac{g_3''}{(g_1 g_2 g_3)}$$

$$d_0 = 1 - \frac{g_3'}{(g_1 g_2 g_3)}$$

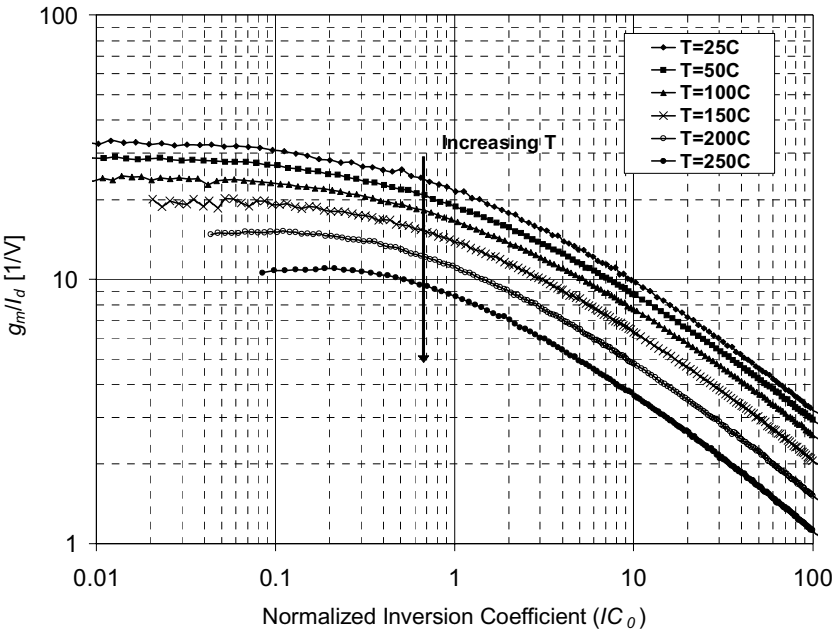
$$d_1 = 1 - \frac{g_3''}{(g_1 g_2 g_3)}$$

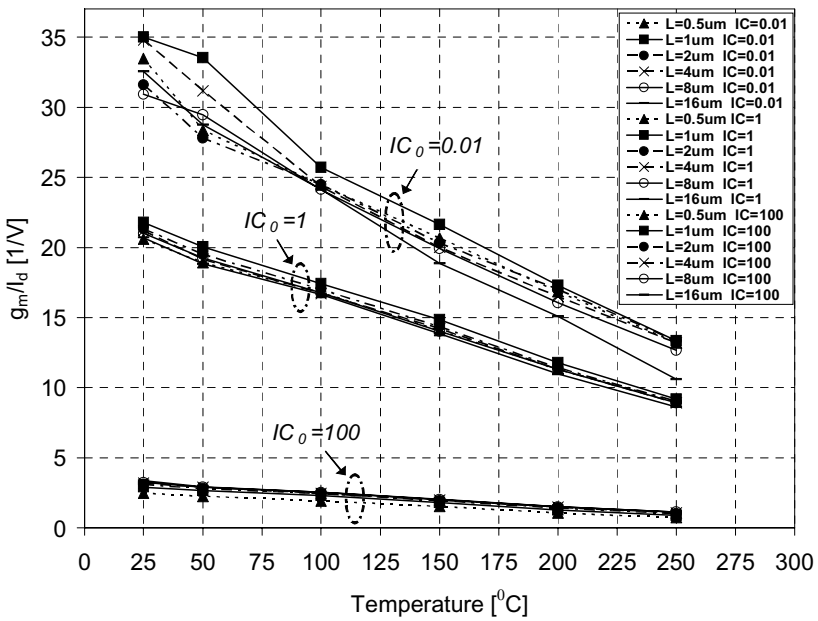
- Implemented as delay, shift, and adder functions
- Coefficients d_0 and d_1 determined by integrator gains

2-2 Cascade Modulator – Switched Capacitor Diagram



Device Characterization Over Temperature Is Critical In High-Temperature Precision Converter Design

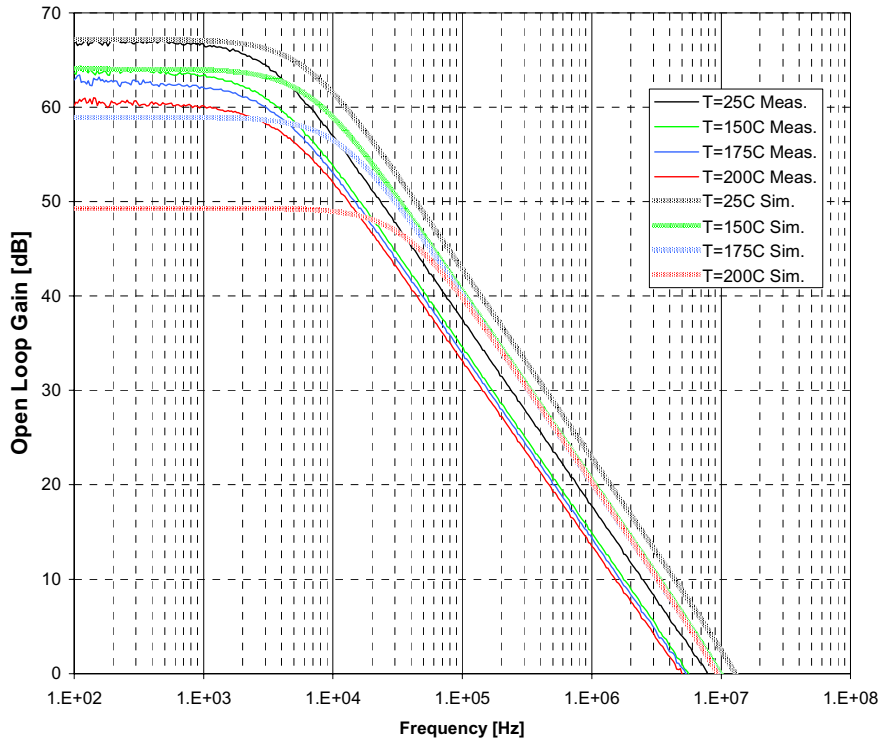




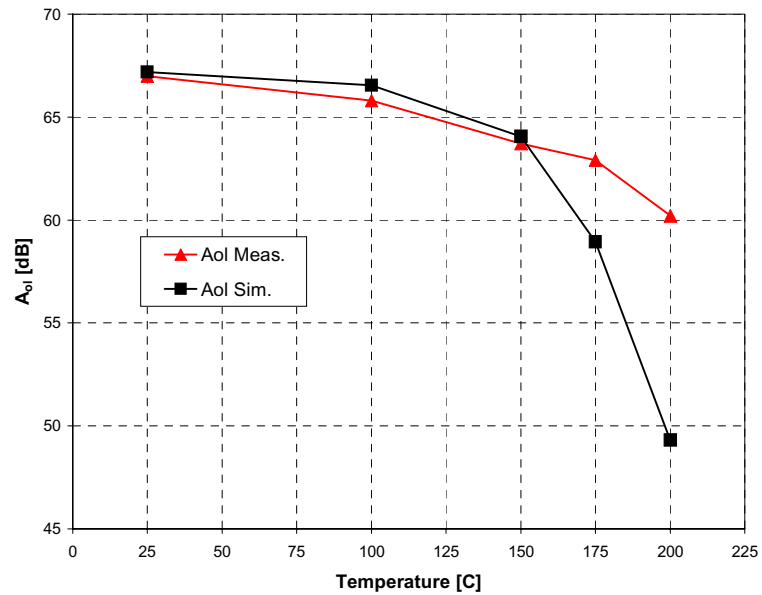
Packaging & Implementation of Support Circuits is a Significant Challenge in High-Temperature Testing

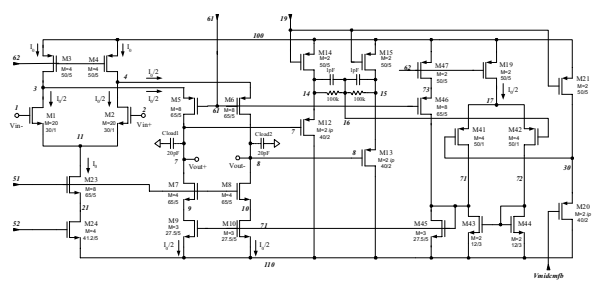
Vendor Supplied Design Models Are Inadequate For High-Temperature Simulations (T>150°C)

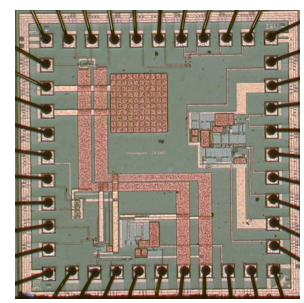
Measured Opamp Open Loop Gain vs. Temperature



Comparison of Measured & Simulated DC Open-Loop Gain







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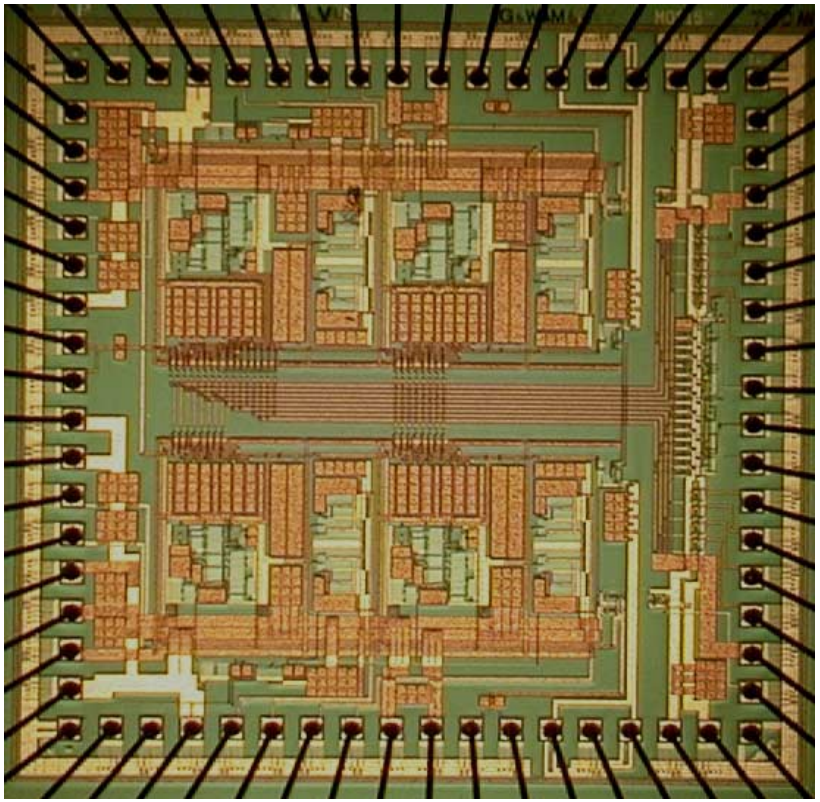
UT-BATTELLE

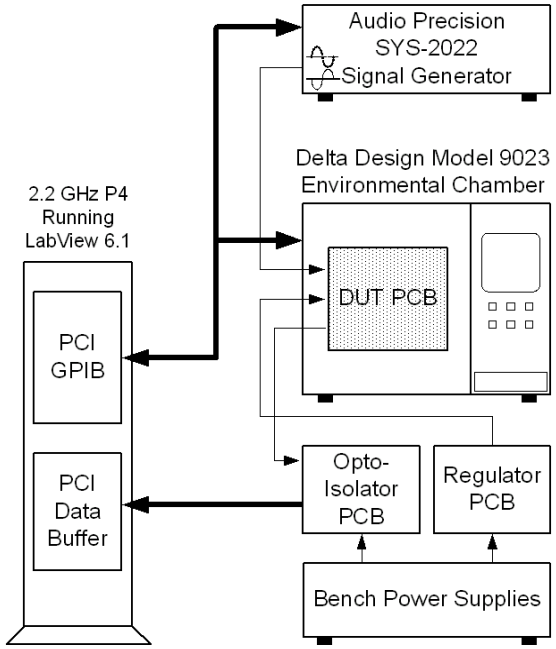
Custom ORNL-Designed 2nd- & 4th-Order ΣΔ Modulator ASIC

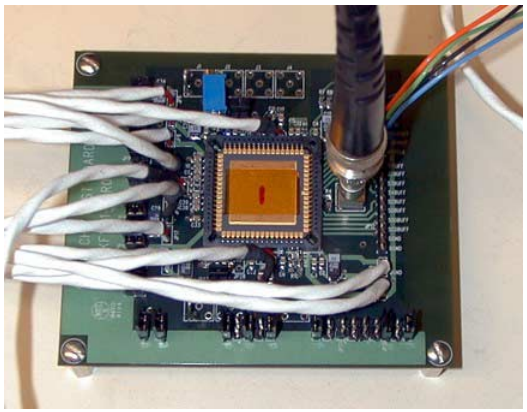


sdmod4_chip
(68-pin J-LDCC Package)

- **Features**
  - 2nd- & 4th-Order Modulators
  - Fully Differential
  - Input Voltage Range ± 0.5V (2V Diff) or ± 0.25V (1V Diff)
  - 3.3V Supply
  - ~ 3.5mm X 3.5mm
  - 0.5μm SOS (Peregrine)

Custom Modulator Test System





Data Acquisition System

- LabView-based Control Program
- Automated Input Signal Amplitude, Frequency, & Temperature Sweeps
- Up to 2048K bits/channel/run (2 channels)
- FFT Display With FFT Averaging
- SNR, SNDR, THD, DR Calculation
- Very Low Distortion Sine Wave Generator
- Instruments Utilize GPIB Interface
- Environmental Chamber (Up to 300ºC)
- Designed for Both Circuit Optimization and Fully Automated Data Acquisition

Performance Parameters Calculated from the Modulator FFT Data

- Signal-to-Noise Ratio (SNR)

$$SNR_{dB} = 20 \cdot \log\left[\frac{V_f}{\sqrt{V_{n1}^2 + V_{n2}^2 + \ldots + V_{nm}^2}}\right][dB]$$

- Signal-to-Noise+Distortion Ratio (SNDR)

$$SNDR_{dB} = 20 \cdot \log\left[\frac{V_f}{\sqrt{V_{n1}^2 + V_{h1}^2 + V_{n2}^2 + V_{h2}^2 + \ldots + V_{nm}^2 + V_{hp}^2}}\right][dB]$$

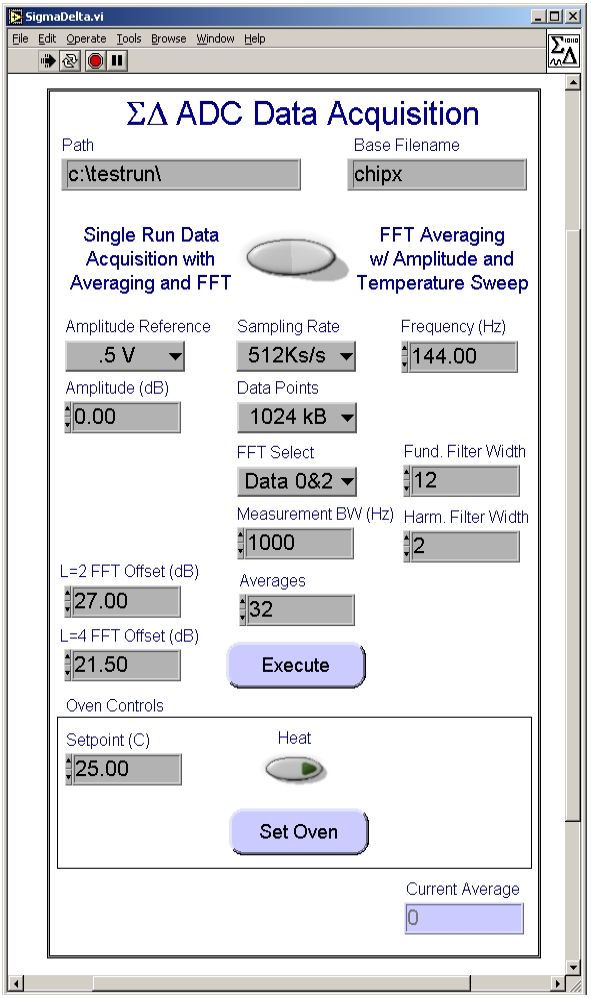
- Total Harmonic Distortion (SNR)

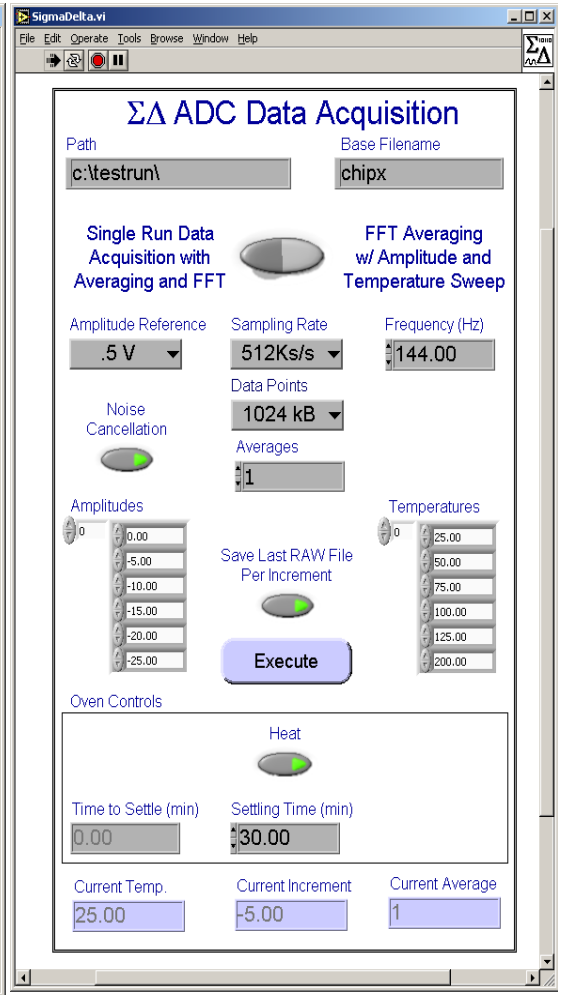
$$THD_{dB} = 20 \cdot \log\left[\frac{\sqrt{V_{h1}^2 + V_{h2}^2 + \ldots + V_{hp}^2}}{V_f}\right][dB]$$

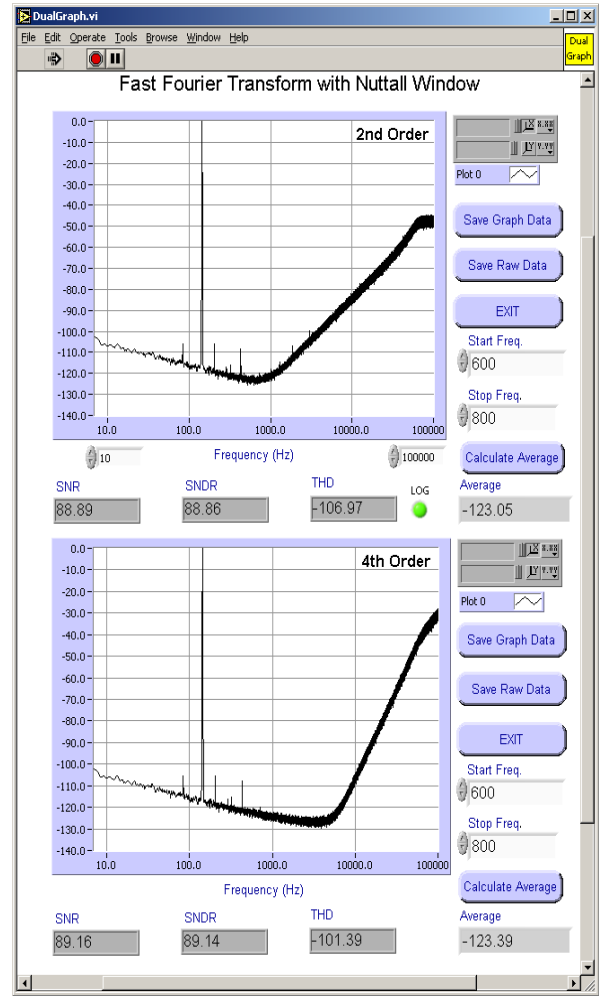
- Dynamic Range (DR)

$$DR_{dB} = 20 \cdot \log\left[\frac{V_{in_{fullscale}}}{V_{in_{SNR=1}}}\right][dB]$$

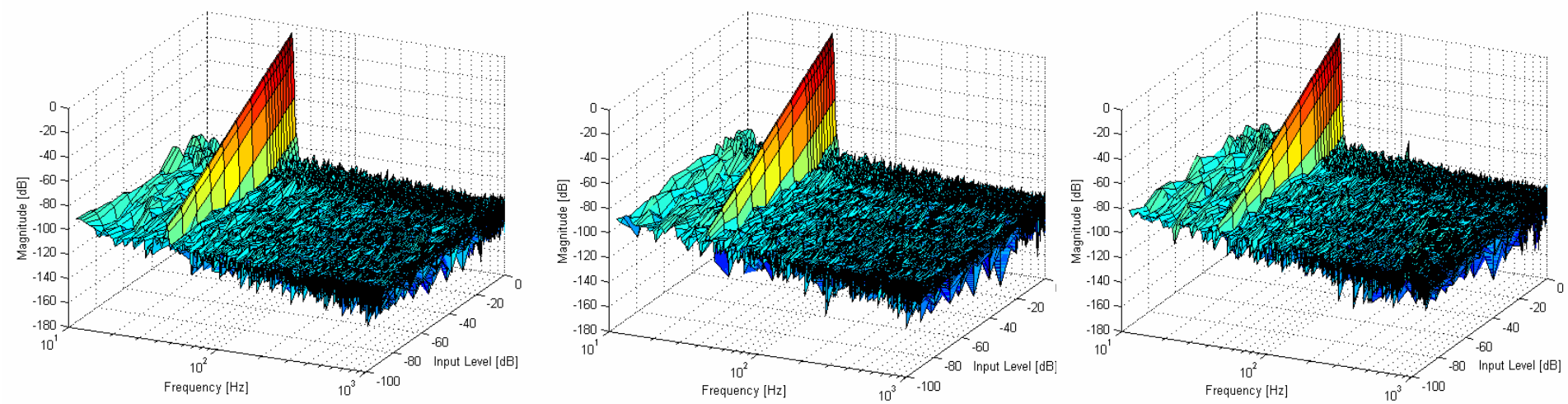
LabView-Based Data Acquisition Software







Measured Modulator Spectra Vs. Temperature (2nd-Order, f_{in}=36.6Hz, chip2)



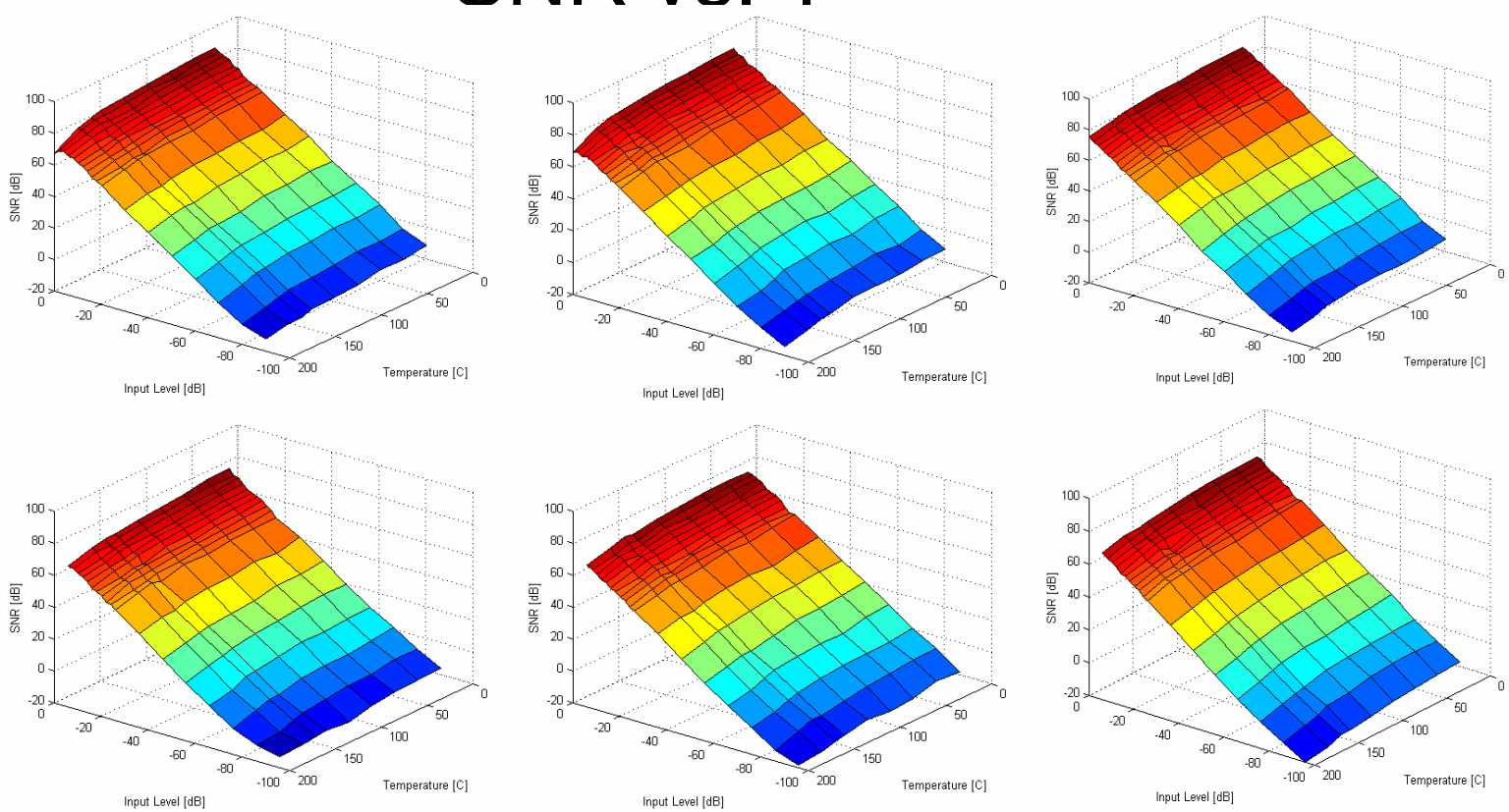
T=25ºC *T=150ºC* *T=200ºC*

- No significant 60 Hz components observed
- Harmonic distortion observed only at high temperature for near full-scale inputs
- Noise floor is 1/f dominated

Modulator Measurement Results – SNR vs. T

2nd Order

4th Order

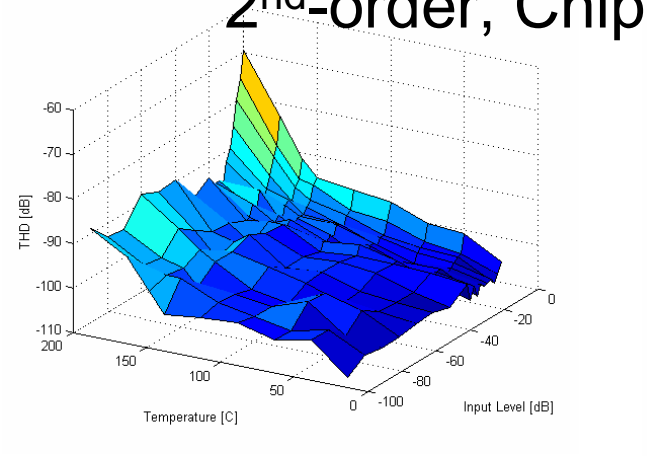


f_{in}=36.6Hz ***f_{in}=144Hz*** ***f_{in}=950Hz***

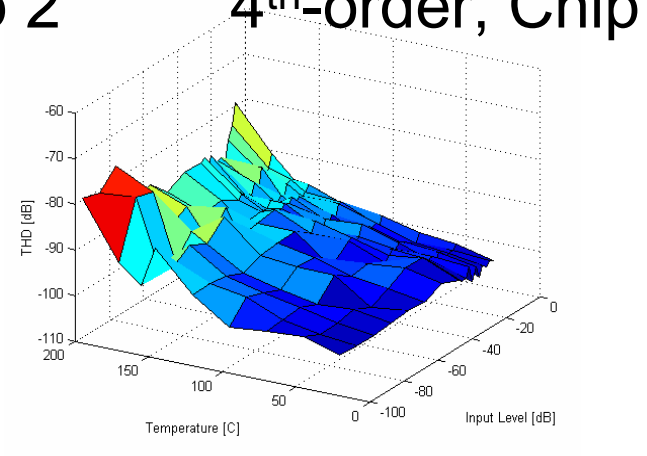
Reduction in SNR with increasing temperature follows increase in noise floor

Modulator Measurement Results - THD vs. T (f_{in}=144Hz)

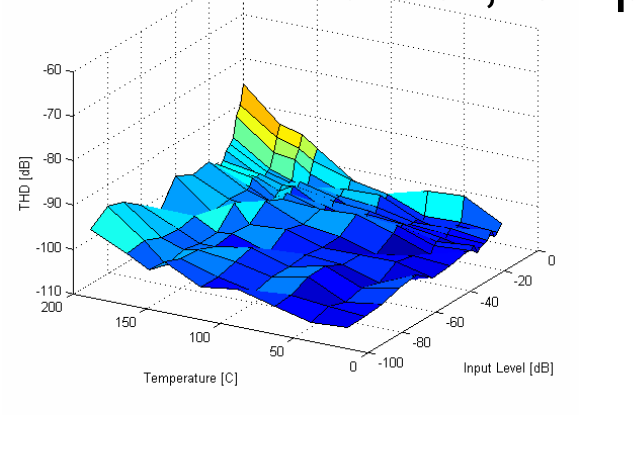
2nd-order, Chip 2



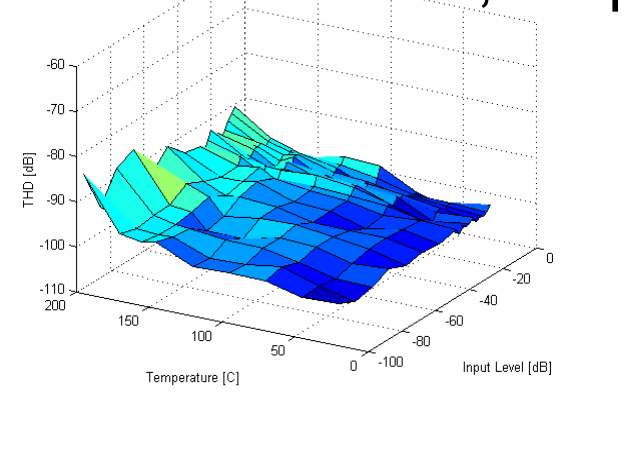
4th-order, Chip 2



2nd-order, Chip 4



4th-order, Chip 4



ΣΔ Modulator Test Summary

Sampling Rate	512kHz
Oversampling Ratio	256
Digital Output Rate	2kS/s
Differential Input Range	2V
Power Dissipation	32.5mW
Active Area	~9mm^2
Technology	0.5µm SOS-CMOS

Parameter	**T=25°C (2nd / 4th)**	**T=150°C (2nd / 4th)**	**T=200°C (2nd / 4th)**
Peak SNR [dB]	92.7 / 92.4	86.9 / 86.9	81.1 / 81.1
Res. [bits]	15.5 / 15.3	14.9 / 14.5	13.5 / 13.3
Peak SNDR [dB]	92.3 / 92.1	86.7 / 86.6	80.6 / 80.6
THD [dB]	-103/ -103	-94 / -99	-90 / -94

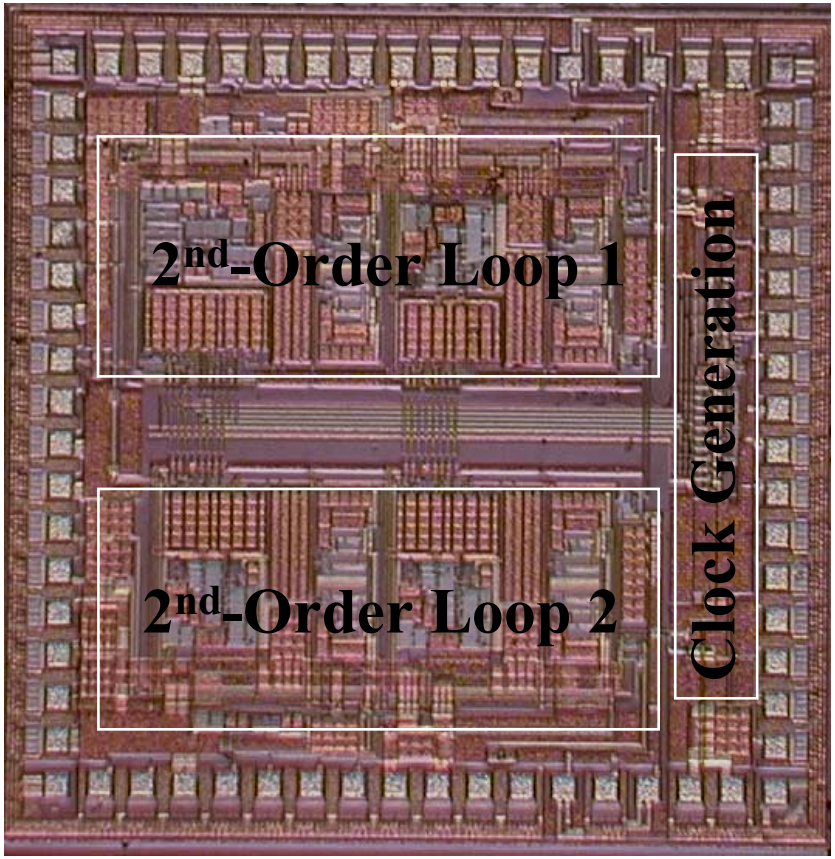
Testing Initiated On Two New ORNL-Designed ΣΔ Modulators

sdmod4_cds1 ASIC

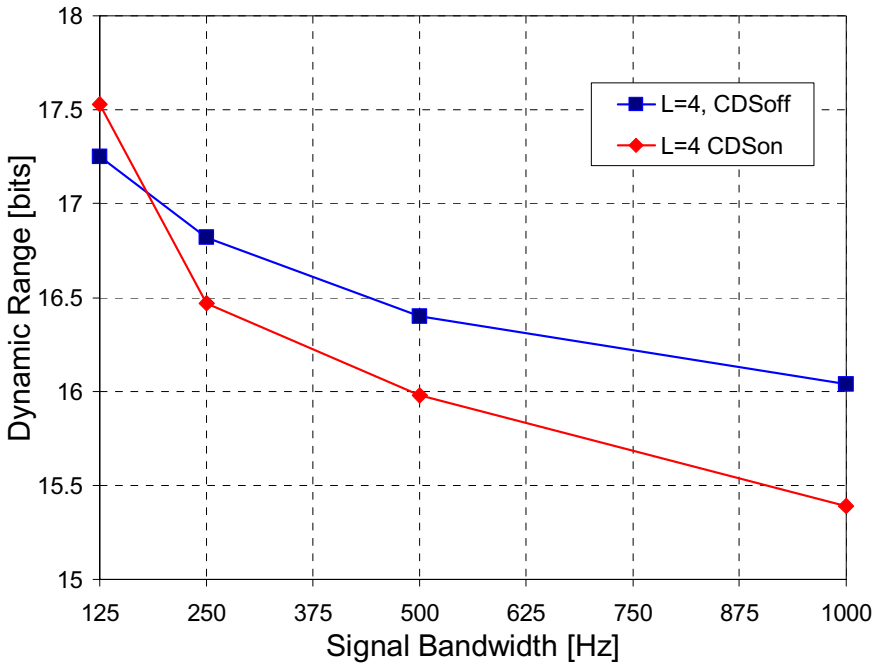
- Low Noise Integrator Amplifier
- 1/f Noise Reduction Method – Correlated Double Sampling (CDS)

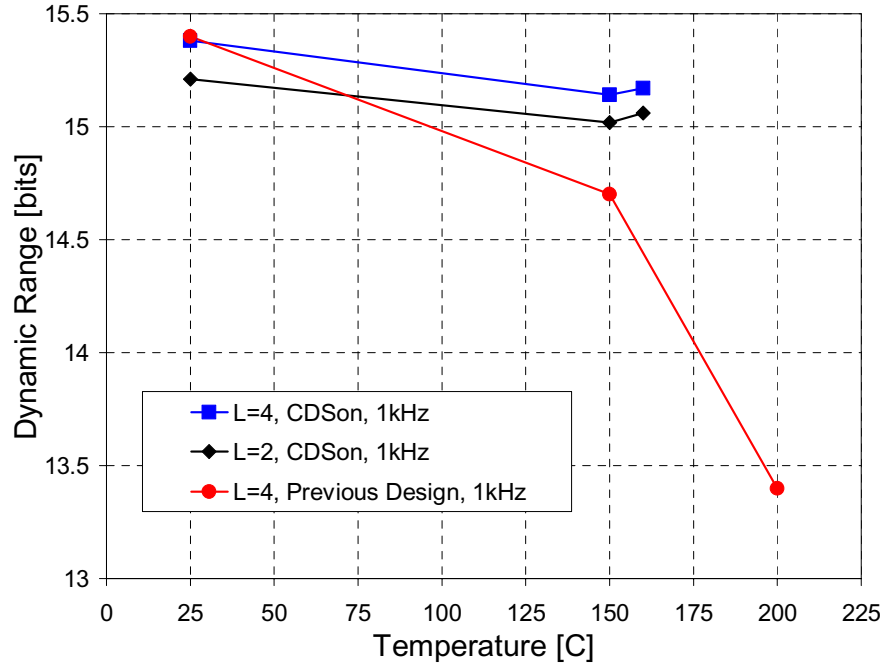
sdmod4_chop2 ASIC

- Low Noise Integrator Amplifier
- 1/f Noise Reduction Method - Chopper



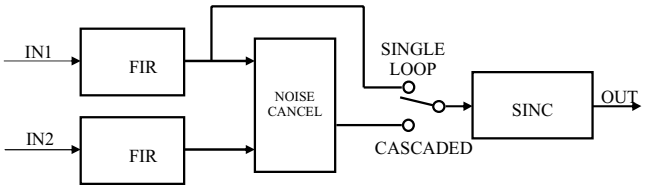
sdmod4_cds1 ASIC
Preliminary Test Results

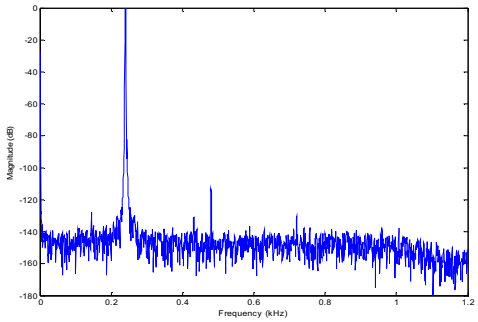




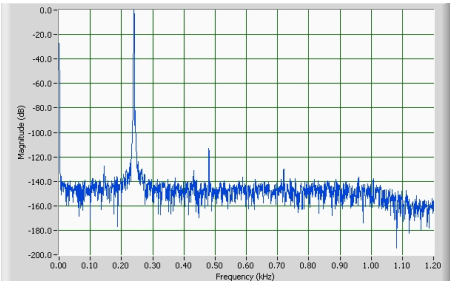
Initial Testing Indicates Significant Improvement In High-Temperature Performance

An SOS Digital Filter Has Been Fabricated And Is Under Evaluation



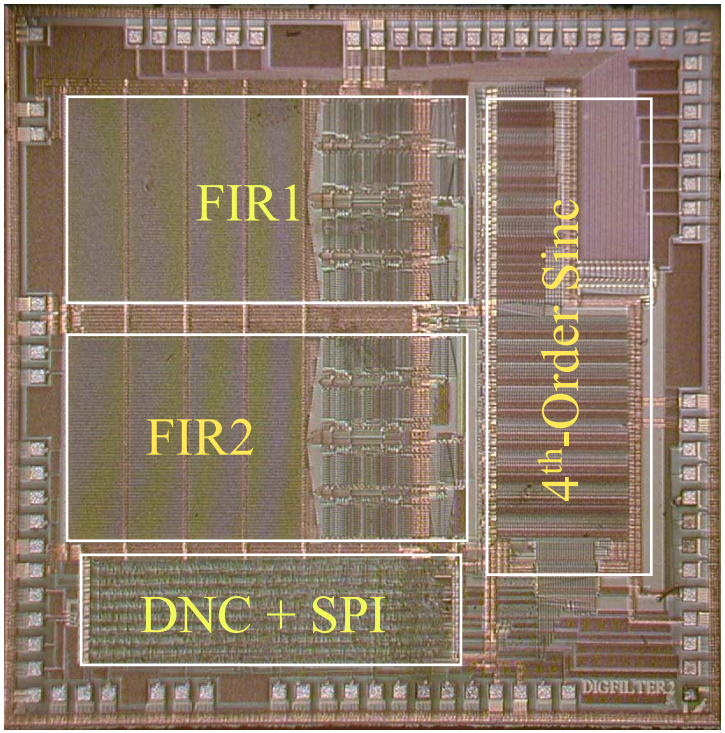


Matlab Simulation with AD1555 Data



FPGA Implementation with AD1555 Data

0.5μm SOS (Peregrine)
~ 5.2mm X 5.2mm



Conclusion

High-Precision Data Conversion at Elevated Temperatures is Attainable With Proper Selection of the ADC Architecture and the IC Fabrication Process

- Select an ADC Topology That Is Tolerant of Temperature-Induced Component/Circuit Errors → $\Sigma\Delta$

- Utilize a Fabrication Technology With Adequate Device Performance & Survivability – SOI/SOS – SiC?

Ongoing Research at ORNL Is Directed Towards Improved High-Temperature Circuits

- High-Precision, Wide-Temperature Voltage References
- High-Temperature Device/Circuit Characterization & Modeling (300°C)
- Improved Tools For ΣΔ Modulator Simulation
- Development of Additional Circuit Functions in SOS/SOI For High-Temperature Applications
- Pursue Collaborations in Si-C Research