Electronics for Diverse Cold Temperatures of Mars

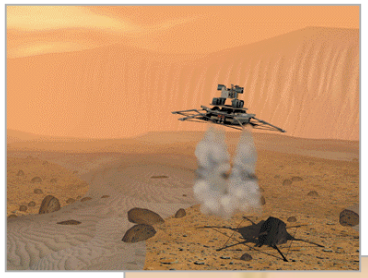
-120 C to 20 C

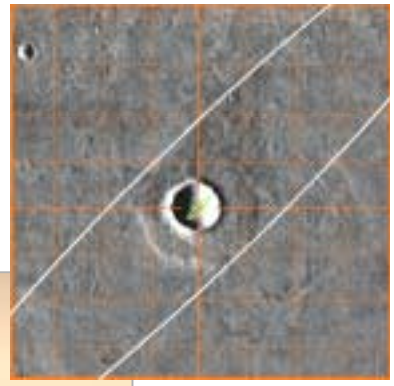
(-120 C to 80 C for electronics next to the actuators and motors)

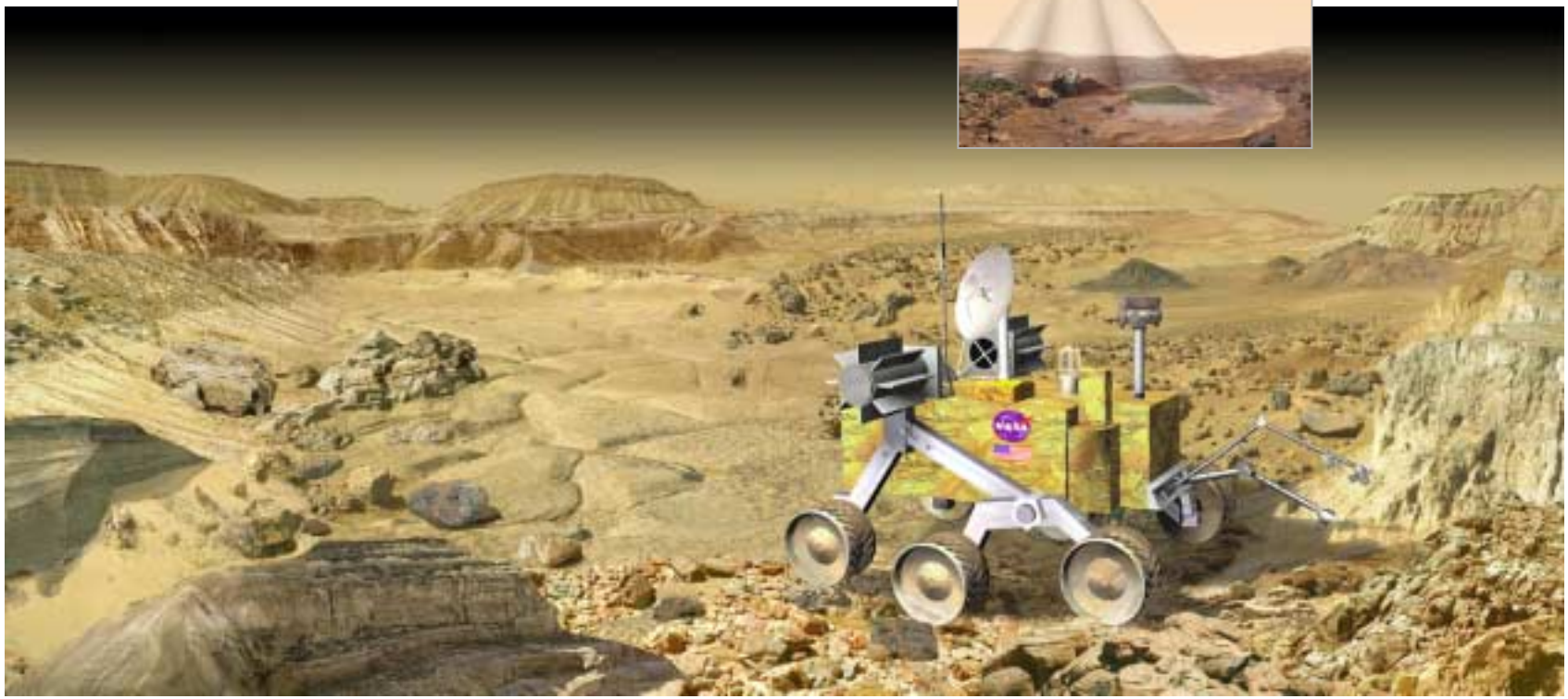
2009 MSL (Mars Science Laboratory)

Carries state of the art in-situ science experiments

- **Central Warm Electronic Box**
- **Distributed Thermal Cycle Resistance Electronics (TCRE) for control of Motors and Actuators**
- **TCRE electronics have to survive 1500 Cycles between –120C and +80C**

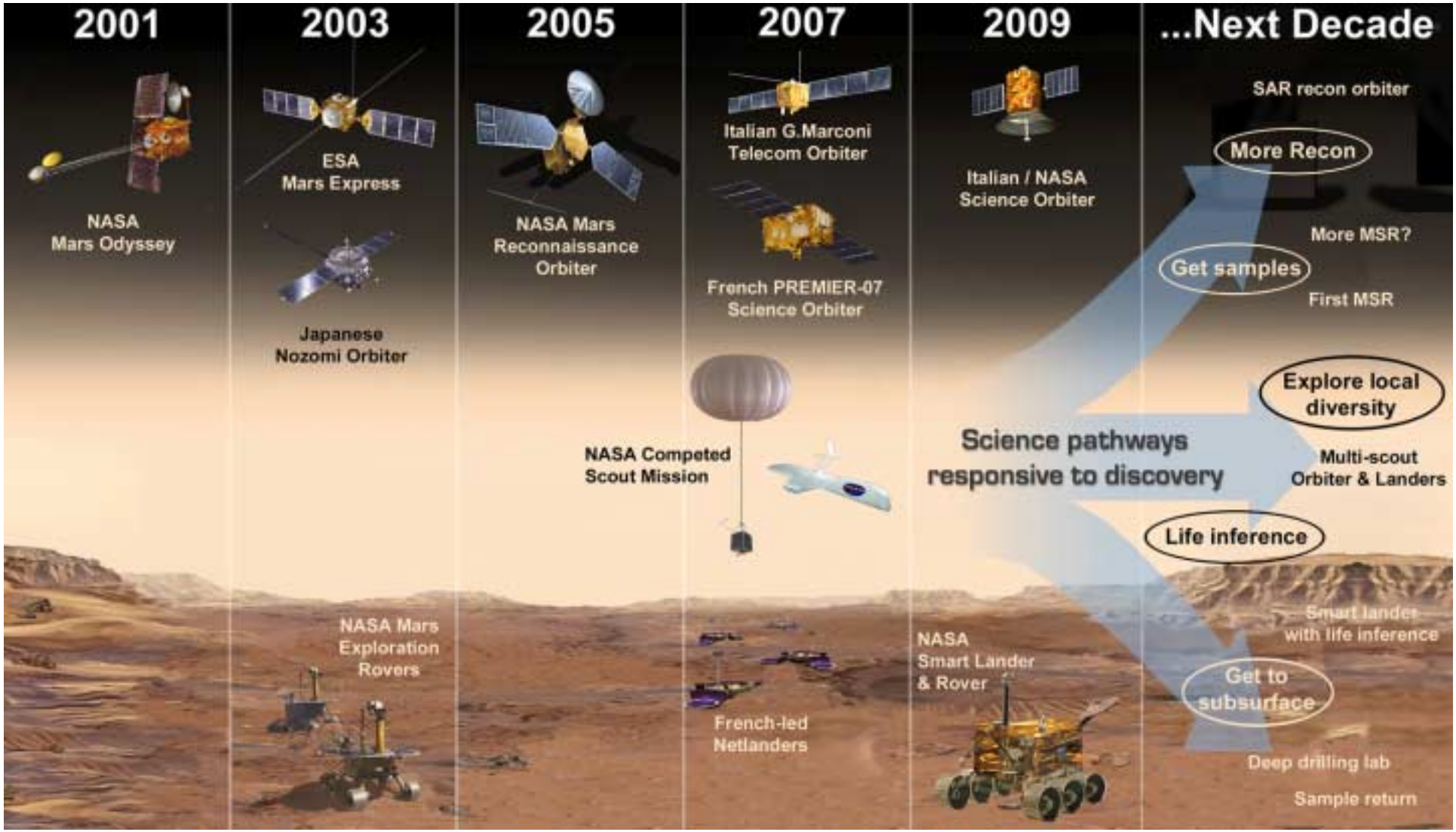






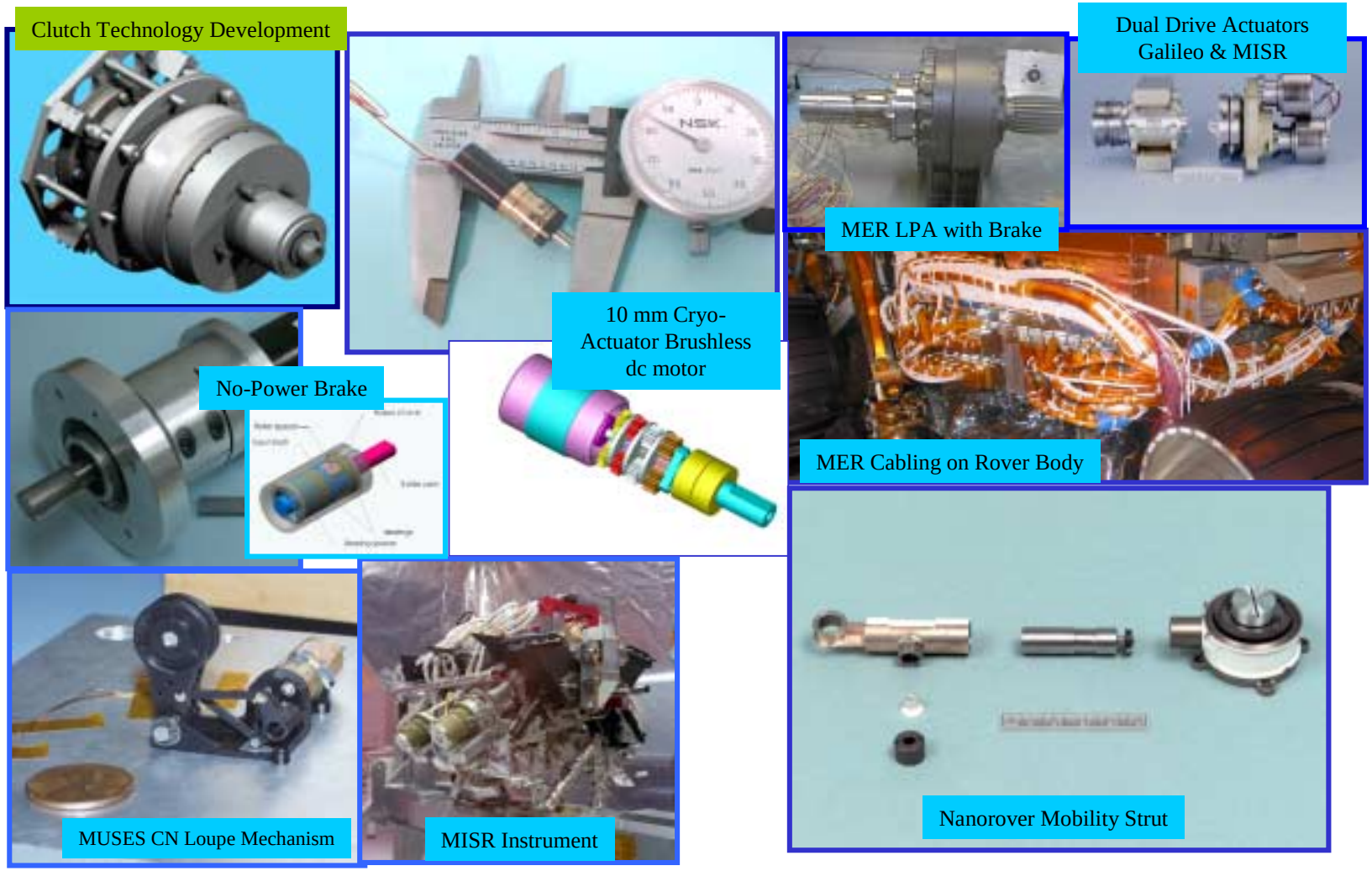
Mars Exploration Program

Launch Year



Motors and Actuators

Some examples of current actuator hardware design



The motor, gearbox, and drive electronics that make up an actuator need to be an integral unit. Motor current drive is 15A max!.

Mars Temperature is outside the Catalog Range of Traditional Electronics

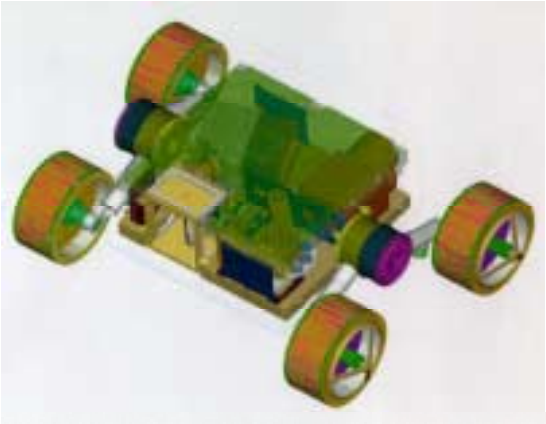
- CMOS works at –120 Deg C. However, traditional components are optimized for terrestrial operating range.

Possible Issues, Digital

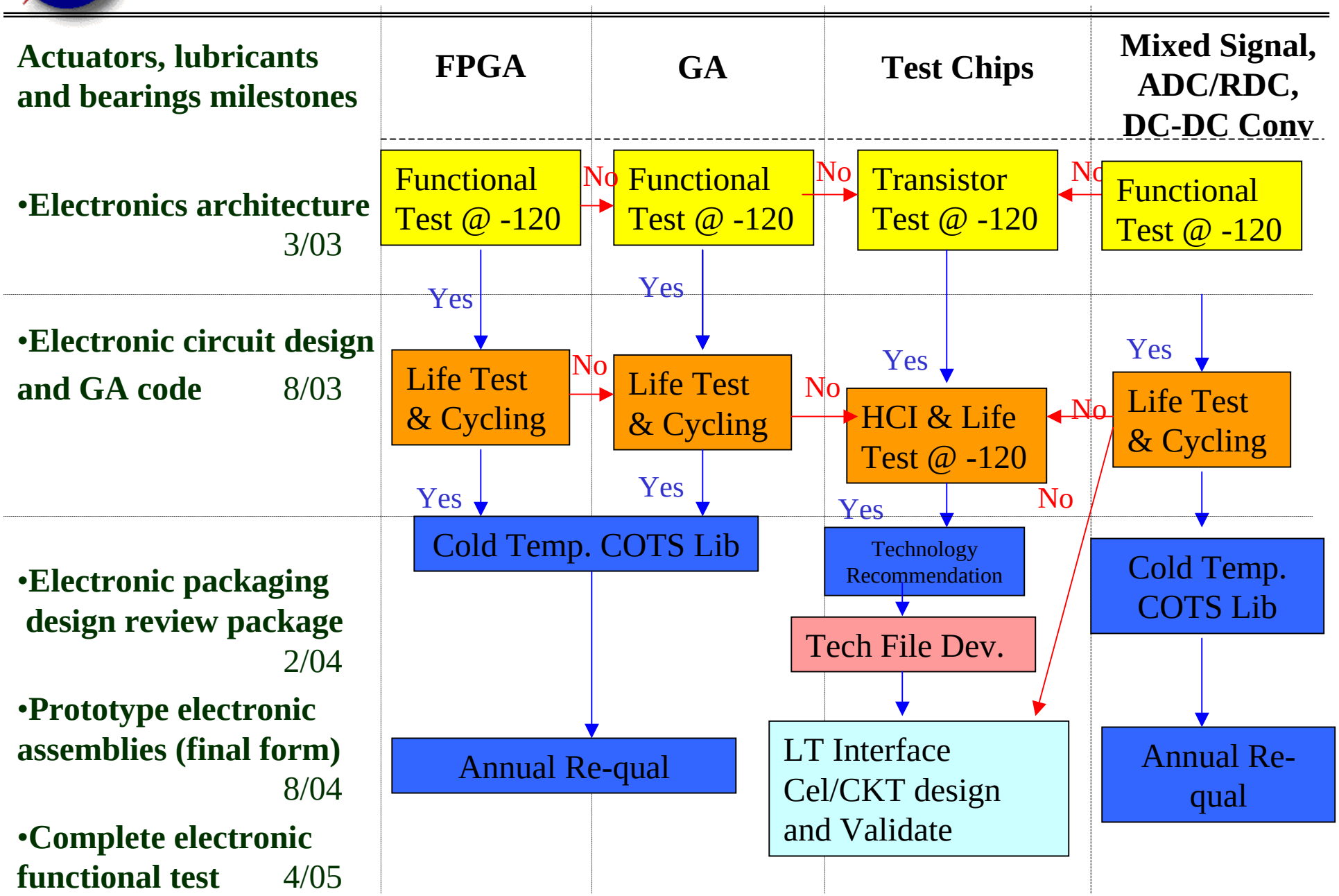
- FPGA vendors: Actel, Xilinx, Altera, TI
  - Clock Tree, Anti Fuse technology , On board RAM, PLL, Setup and Hold times, HCI, …
- GA vendors: Honeywell, Samsung, National Semi, LSI Logic
  - HCI, Setup and Hold times,…

Possible Issues, Analog (ADC and RDC)

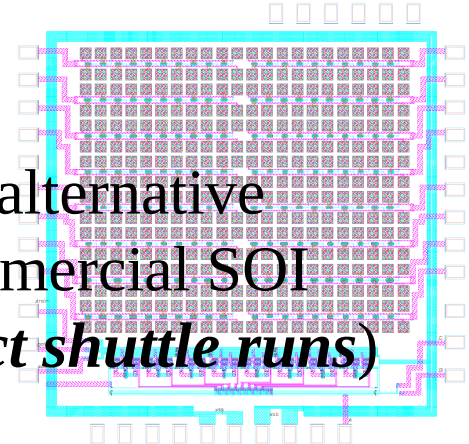
- Muses CN Experience with 12 bit (7882RP) ADC
  - Functional at –120 C
  - No long term life test
  - Large power consumption
- Very little data on LT RDC's



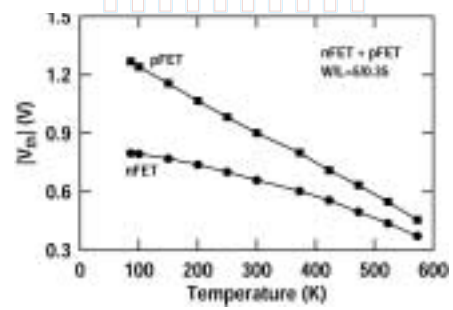
Work Flow/ Decision Tree

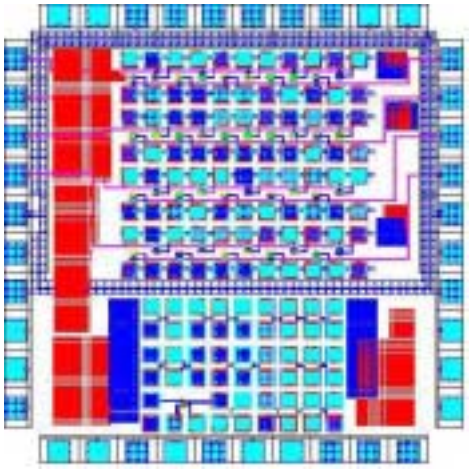


A commercial CMOS IC technology for TCRE for MSL



- Leverage test existing chips fabricated
- Fabricate and characterize additional test chips in alternative commercial CMOS technologies (Honeywell commercial SOI CMOS, TSMC bulk CMOS, ***all offer multi project shuttle runs***)
- Characterization including life test at –120 deg C.
- Compare the results and make recommendation.



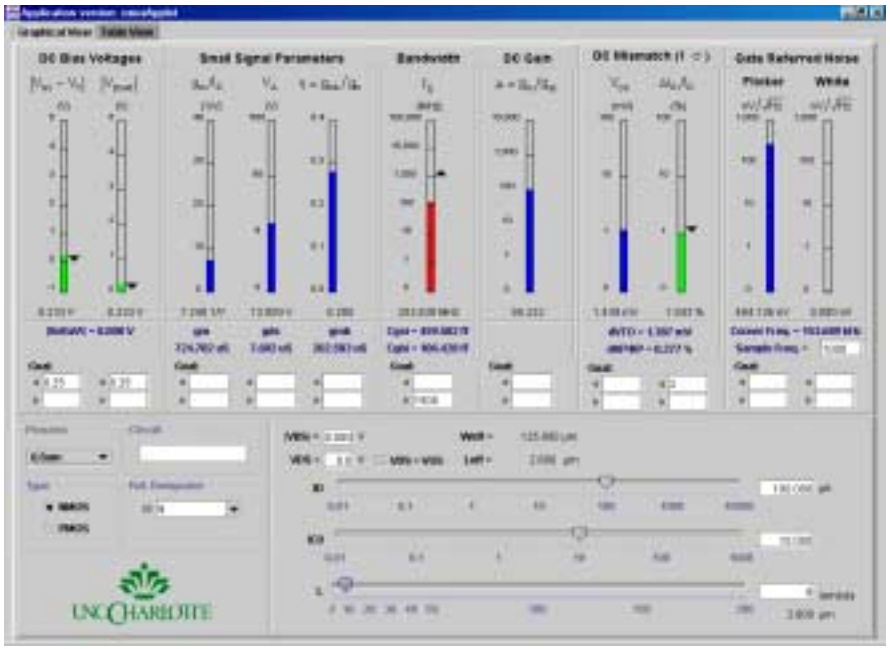


List of tests

- HCI
- R body, SOI
- Noise – flicker (1/f)
- Breakdown voltage
- Latch/snapback
- History and transient effects
- Edge effects
- History effects
- Frequency performance
- Ring osc
- Op amps
- Passives Tc, Vc
- ADC test structure?
- Resolver (RDC)?

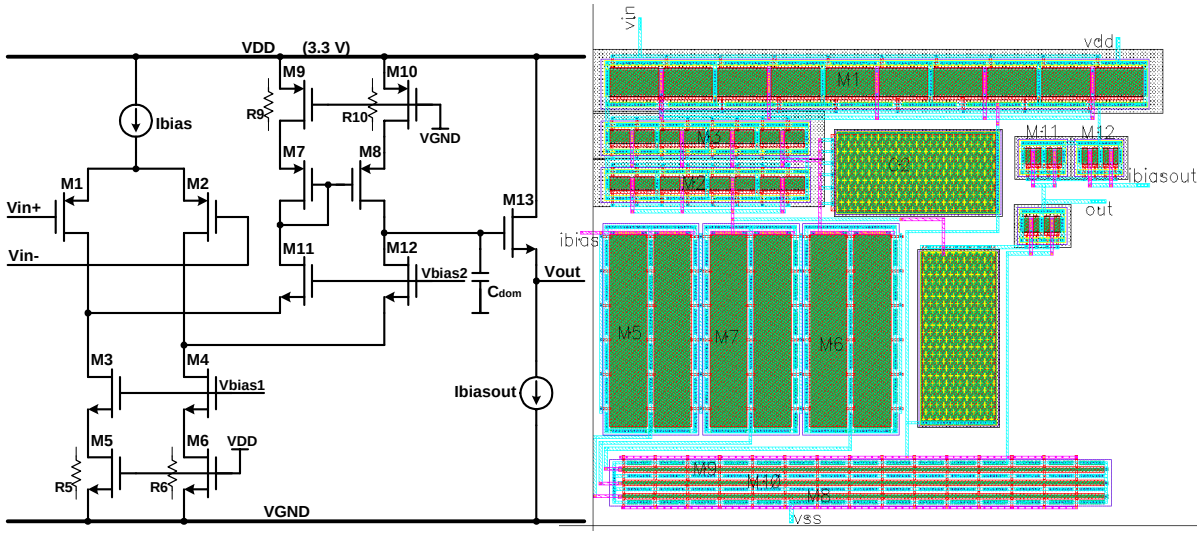
Technology files for wide cold temperature IC development

- Examine the test chip to extract Spice parameters at –120 and ….
- Examine characterization and life test results to develop a set of design rules, which complement the commercial rules and adapt them for wide cold temp design
- Convert the rules into CAD tech files



Develop a set of interface building blocks

- Define a list of enabling building blocks and set of performance matrices (Bandgap ref gen, operational amp, current source,…)
- Design and simulate the blocks using the developed technology files
- Fabricate, and characterize the test chips
- Compare the results with the performance matrix and iterate.
- Update technology files



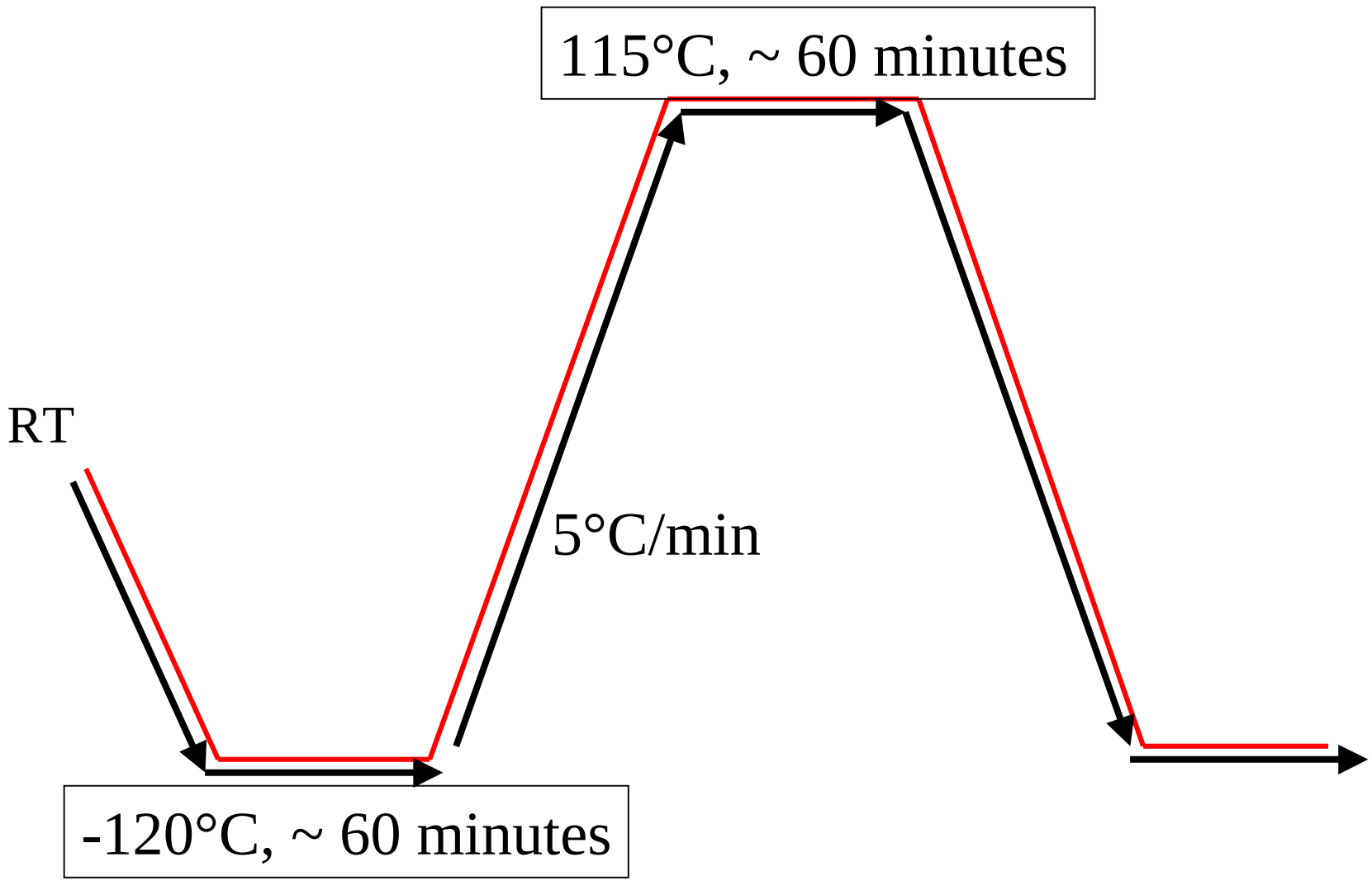
Potential Issues, Packaging

- Thermal cycling
  - Temperature range
    - -120°C to +20°C
    - Range less than typical military range
      - -65°C to +125°C
    - However, zero stress state established at (or near) assembly temperature
  - Number of cycles required – 1500
    - Greater than typical military but on lower end of underhood automotive
- Brittle behavior of materials at low temperature
  - Particularly polymers

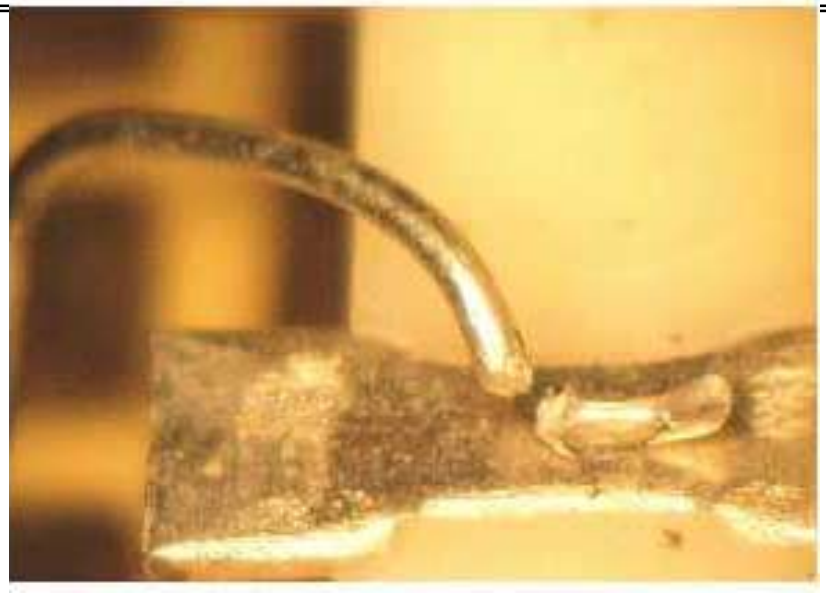
More Questions, Packaging

- Wiring complexity/packaging density
  - Helps determine substrate technology
- Power dissipation
  - Assumed low, but…….
- Number of passive components
  - Do embedded passives make sense?
- Availability of bare die
  - Wire bond
  - Flip chip
    - Die bumping???
    - Chip size???
    - Outgassing issues???
- Hermetic packaging????

Extreme Cold Thermal Cycle Profile (-120/115°C)



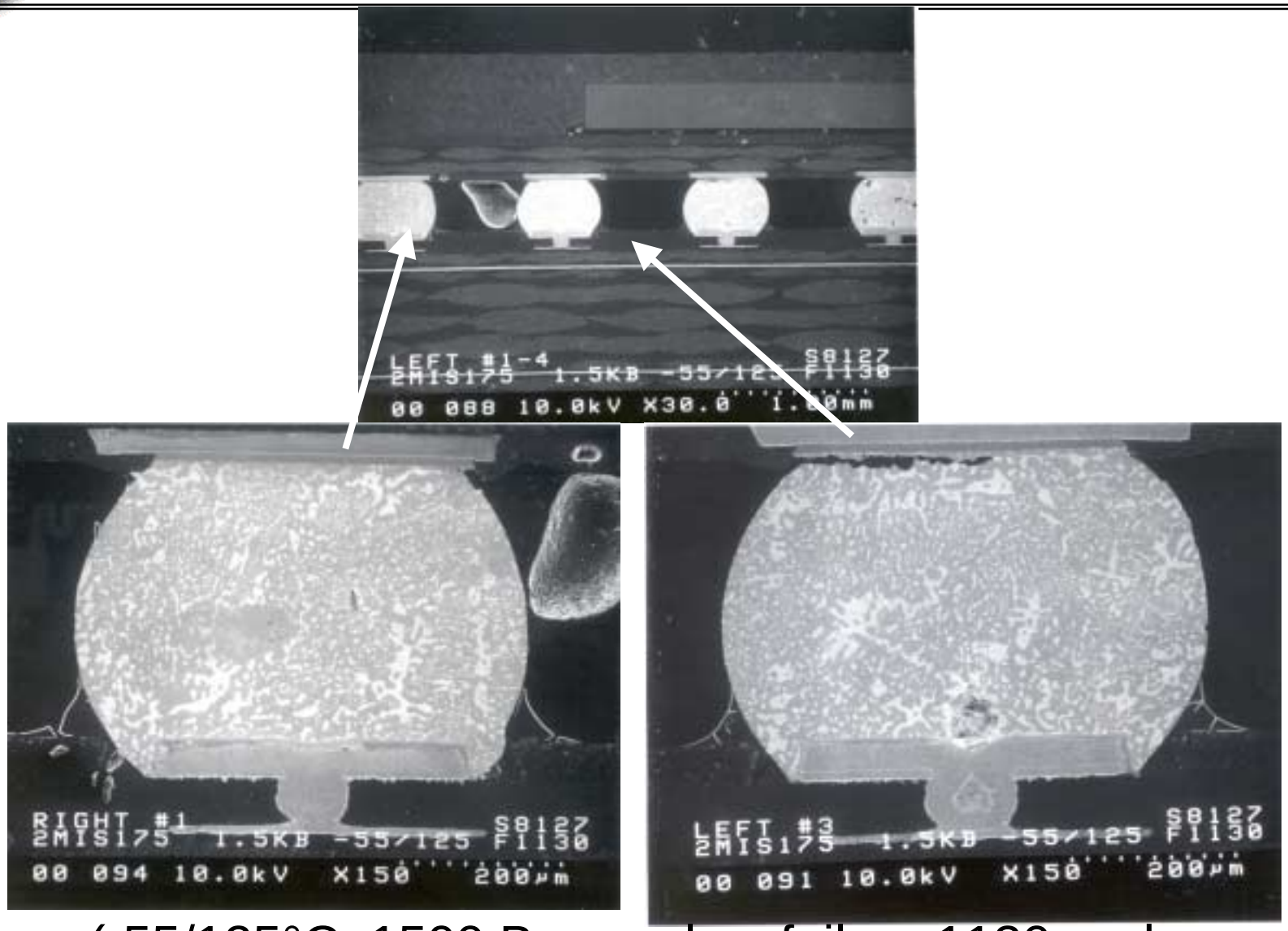
Wire flexure fatigue



- Power and temperature cycling produce cyclic thermo-mechanical stresses which can lead to wire fatigue failure.
- The stresses arise due to the differential expansion of the wire, the chip, and the substrate causing the wire to flex.
- Flexural stresses concentrate at the heel of the wire on the chip side which experiences greater temperature excursion.
- Leads to intermittents, and open circuits.

G. Harman, Wire Bonding in Microelectronics: Materials, Processes, and Yield, McGraw-Hill, New York, 1997.

Solder Failure at the Die Edge/FPBGA



(-55/125°C, 1500 Bng cycles, failure 1130 cycles