# High Temperature Packaging Technology, Passives, and Reliability

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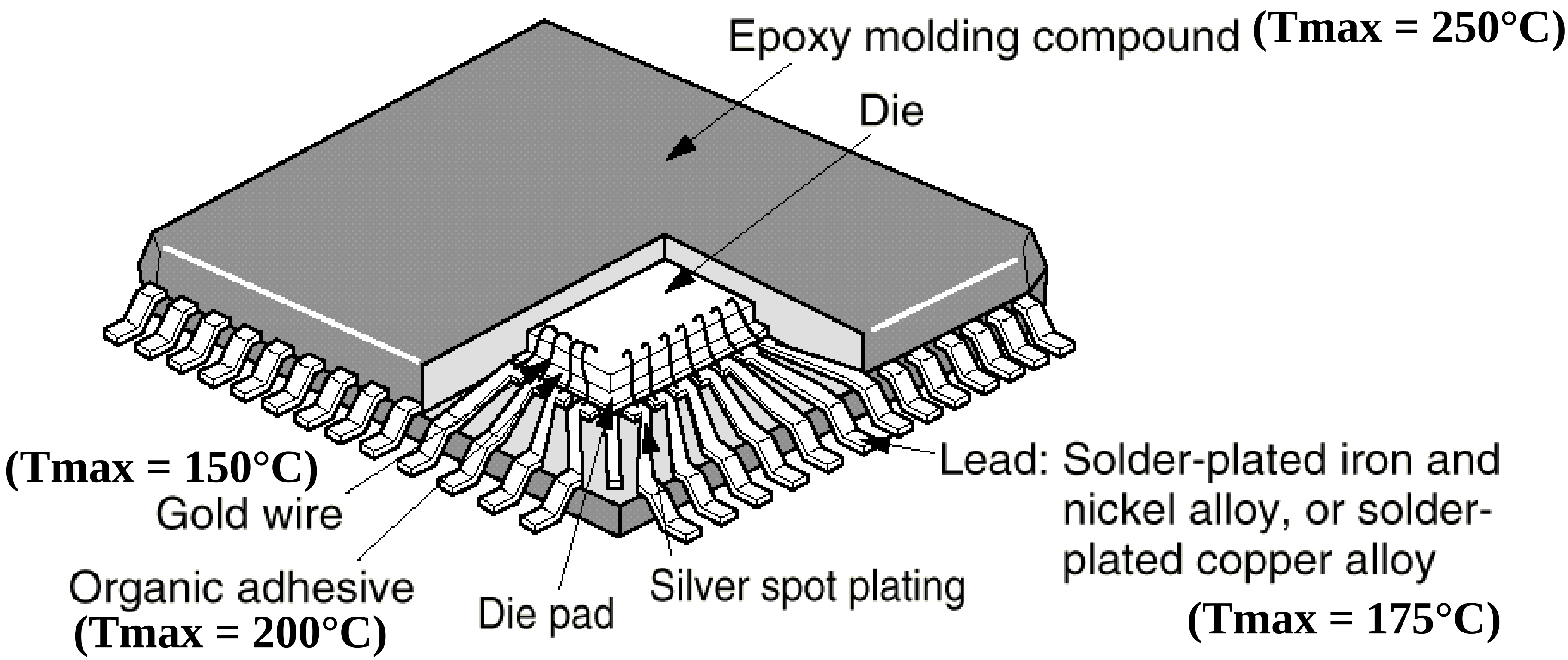
# Acknowledgments

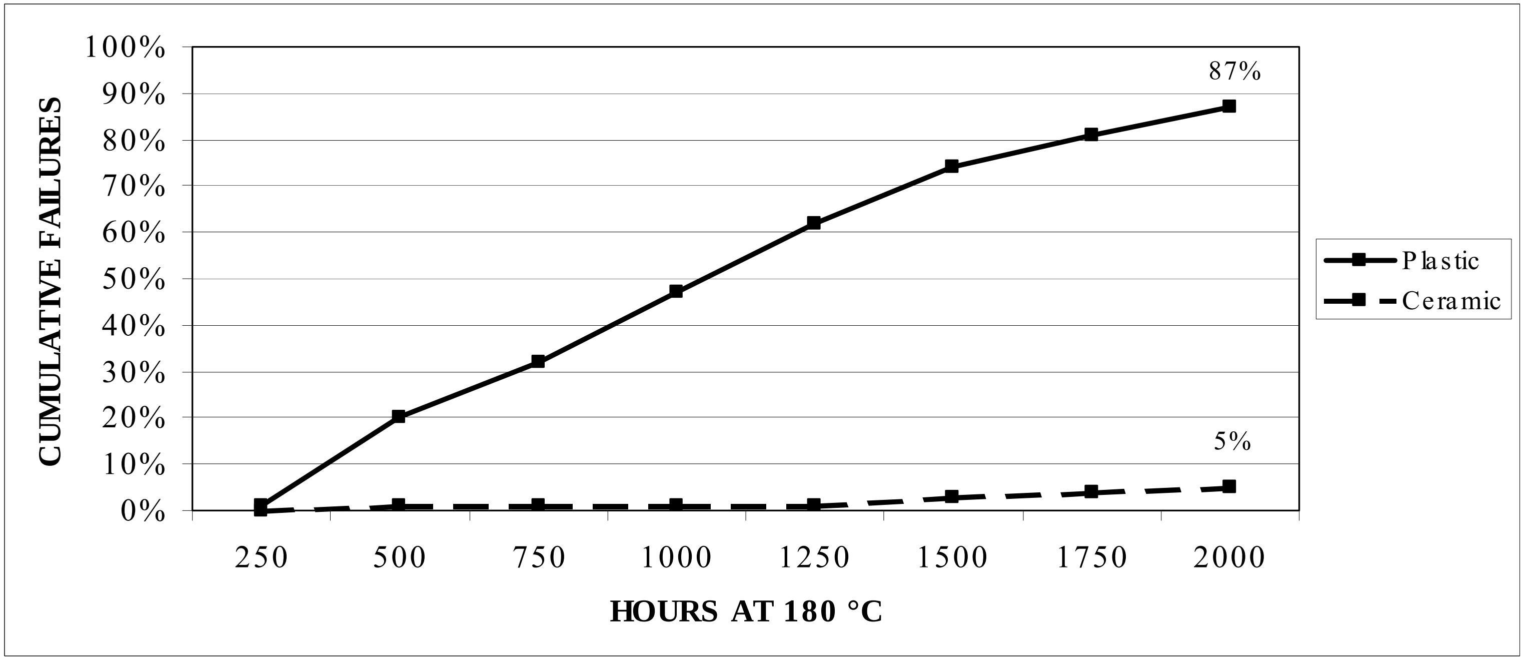

- Dr. LiangYu Chen, NASA Glenn Research Ctr.
- Dr. Abhijit Dasgupta, Univ. of Maryland
- Dr. Rich Grzybowski, Corning, Inc.
- Dr. Wayne Johnson, Auburn University
- Dr. Marjorie Natishan, Phoenix Technologies
- Dr. Michael Pecht, Univ. of Maryland
- DARPA HiTEC Consortium
- CALCE Consortium
- My graduate students

# Temperature limitations of commercial component packaging



# PEMs Fail Faster in Steady State Aging at 180°C

| Test Conditions | Plastic Failures (of 144) | Ceramic Failures (of 136) |
|---|---|---|
| 180 °C Steady State | 123 | 7 |
| 180 °C Cyclic | 8 | 4 |
| 155 °C Steady State | 2 | No Failures |
| 155 °C Cyclic | 1 | No Failures |




**F. P. McCluskey,** K. Mensah, C. O'Connor, A. Gallo, "Reliable Use of Commercial Technology in High Temperature Environments," **Microelectronics Reliability, Vol. 40,** pp. 1673-1680 (2000).

# Intermetallic formation is the dominant failure mechanism

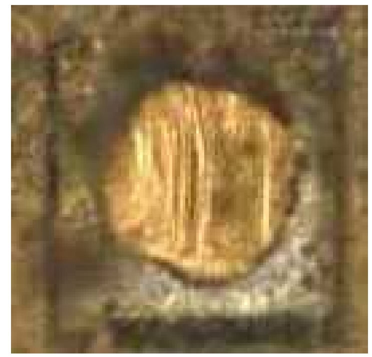
## Microcontroller 180 ºC steady-state

| Failure No. | Time (hrs) |
|---|---|
| 1 | 288 |
| 2 | 315 |
| 3 | 335 |
| 4 | 357 |
| 5 | 360 |
| 6 | 383 |
| 7 | 395 |
| 8 | 408 |

Exposure Time: None

Bond Shear Strength:

74 ± 10 gF



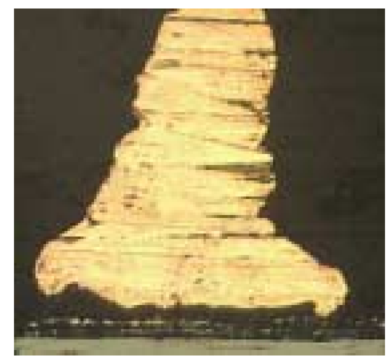
Exposure Time: 451 hrs

Bond Shear Strength:

Sample A 7.0 ± 1.6 gF

Sample B 4.4 ± 2.9 gF

Sample C 6.2 ± 2.2 gF



**F. P. McCluskey,** K. Mensah, C. O'Connor, A. Gallo, "Reliable Use of Commercial Technology in High Temperature Environments," **Microelectronics Reliability, Vol. 40,** pp. 1673-1680 (2000).

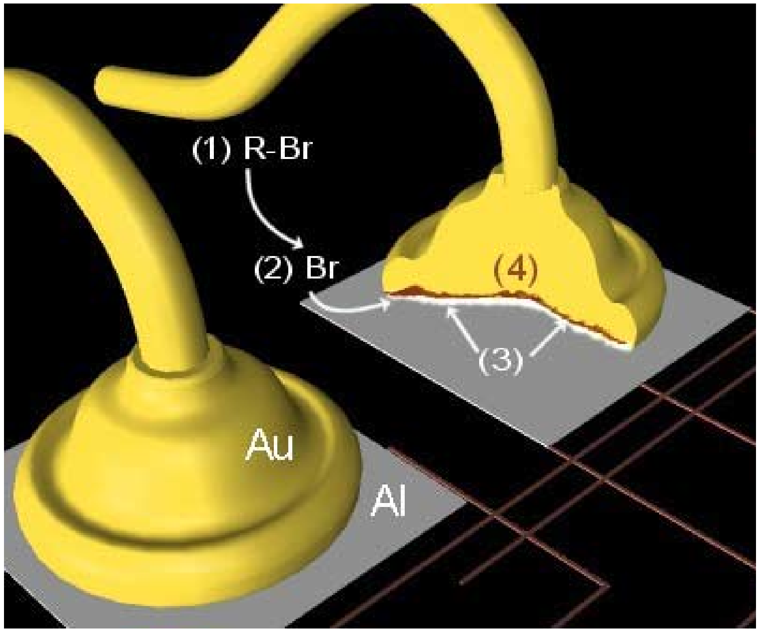
# Intermetallic Degradation Mechanism

## 1. Resin Decomposition

- $RBr \rightarrow HBr + R$
- $HBr + H_2O$ (trace moisture) $\rightarrow H_3O + Br$

## 2. Bromine Diffusion

- Br (resin) → Br (bond interface)




## 3. Intermetallic Formation

- $5Au + 2Al \rightarrow Au_5Al_2$
- $Au_5Al_2 + 3Au \rightarrow 2Au_4Al$

## 4. Chemical Reaction

- $Au_4Al + 3Br \rightarrow AlBr_3 + 4Au$
- $2AlBr_3 + 3O \rightarrow Al_2O_3 + 6Br$

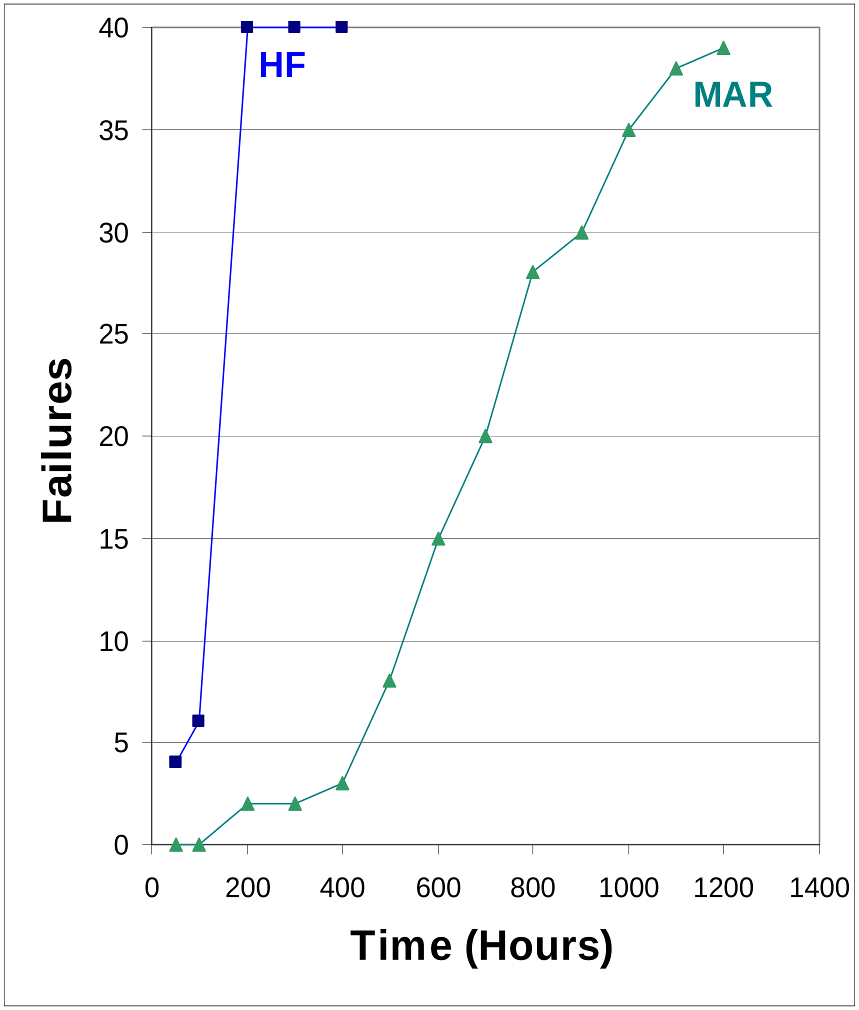
Rate limiting step has been identified as bromine diffusion

# Alternate Flame Retardants

- Higher filler content, low flame retardant (HF)
- Multi-Aromatic Resins (MAR) "Green" Molding Compound
- Transition metal oxides
- Metal hydrate
- Phosphorus based compounds

# Failure Statistics

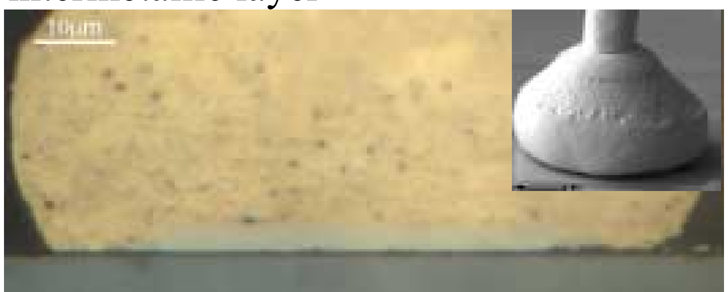
HF vs MAR @ 200 °C




- HF: Complete failure observed after only 200 hours.
- HF: Not suitable for applications at 200 °C.
- MAR: First failures at 200 hours.
- MAR: Complete failure at 1200 hours.

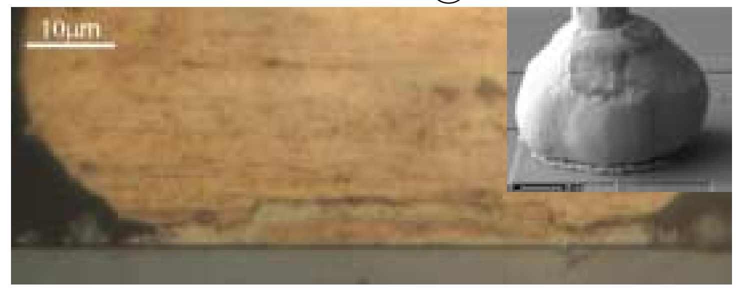
# Intermetallic Growth (Cross Section & SEM)

Initial bond: no exposure, uniform intermetallic layer

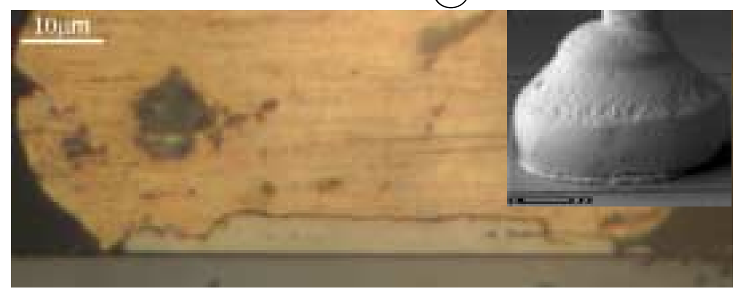



Worst Case

HF-200°C: bond failure @ 300 hours

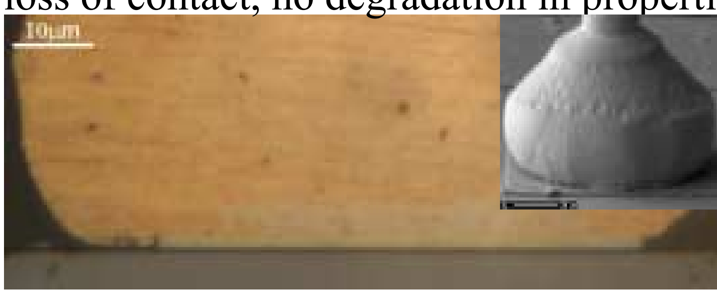



HF-180°C: bond failure @ 500 hours

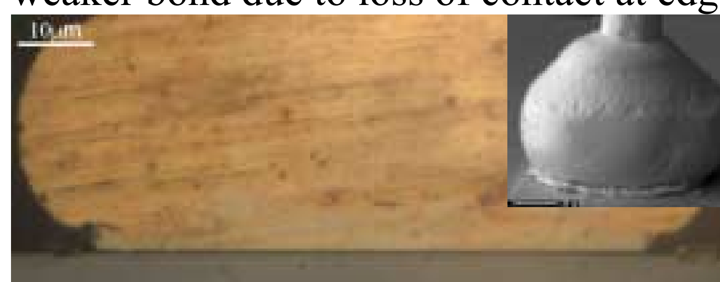



Best Case

MAR-180°C: Intermetallic growth, but no loss of contact, no degradation in properties

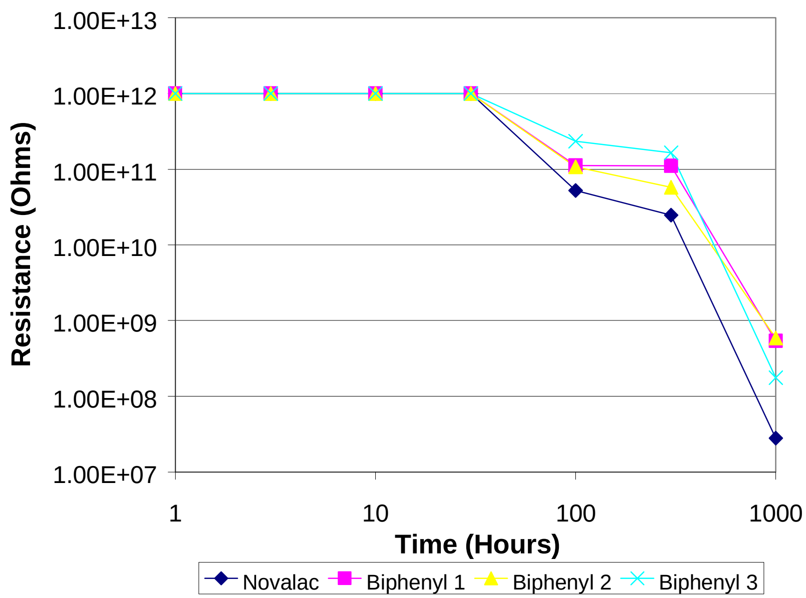



MAR-200°C: 500 hours, higher resistance, weaker bond due to loss of contact at edges

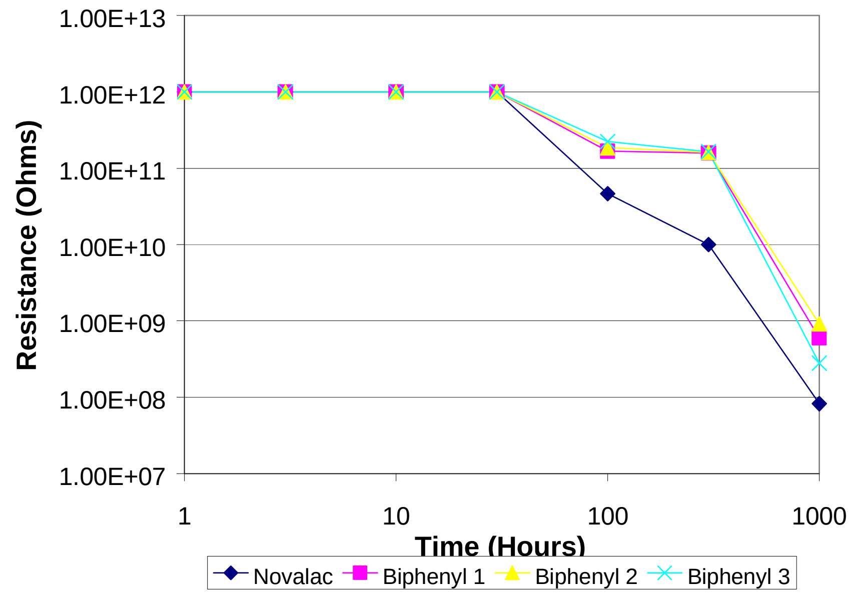


# Encapsulant degrades substantially at 250°C

## 84 lead PQFP leadframes with no die encapsulated in molding compound




Adjacent Leads at 250C




Non-Adjacent Leads at 250C

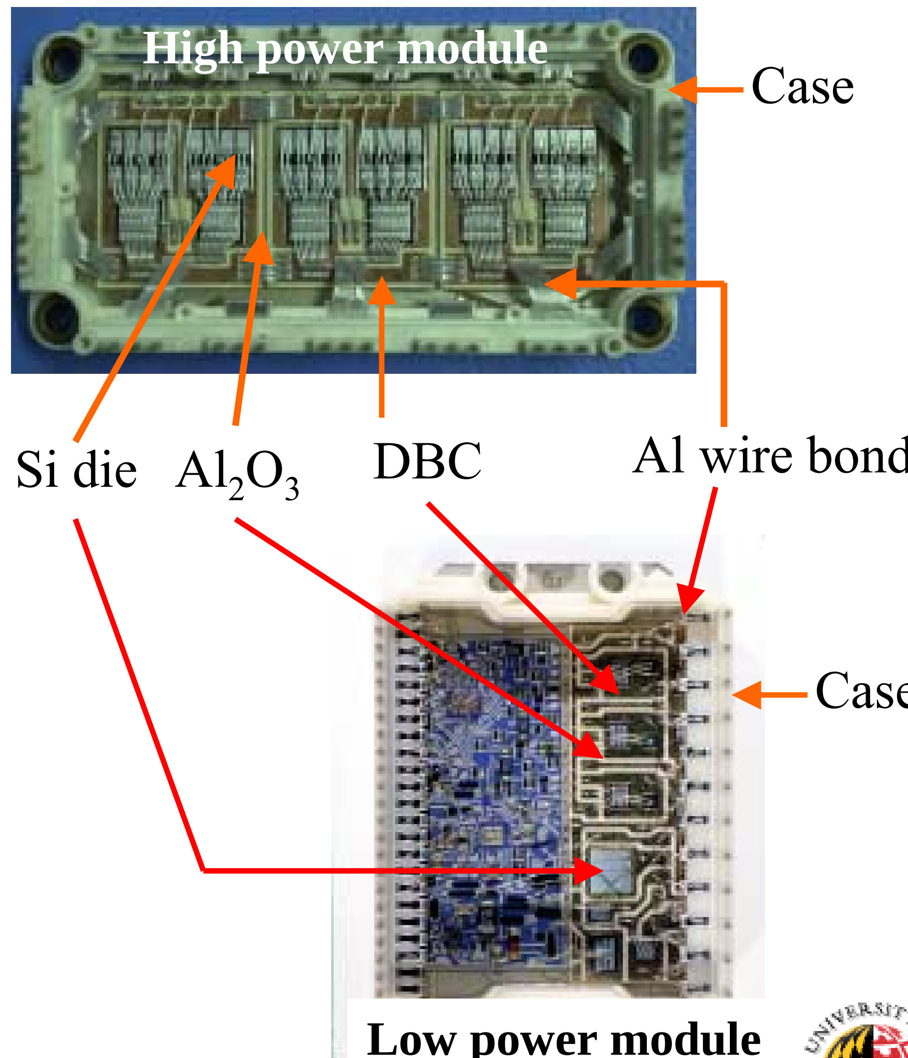
Novalac: 71% $SiO_2$ filler in epoxy cresol novalac
Biphenyl: 84% $SiO_2$ filler in epoxy biphenyl

**F. P. McCluskey,** K. Mensah, C. O'Connor, A. Gallo, "Reliable Use of Commercial Technology in High Temperature Environments," **Microelectronics Reliability, Vol. 40,** pp. 1673-1680 (2000).

# Ceramic Hybrid Modules

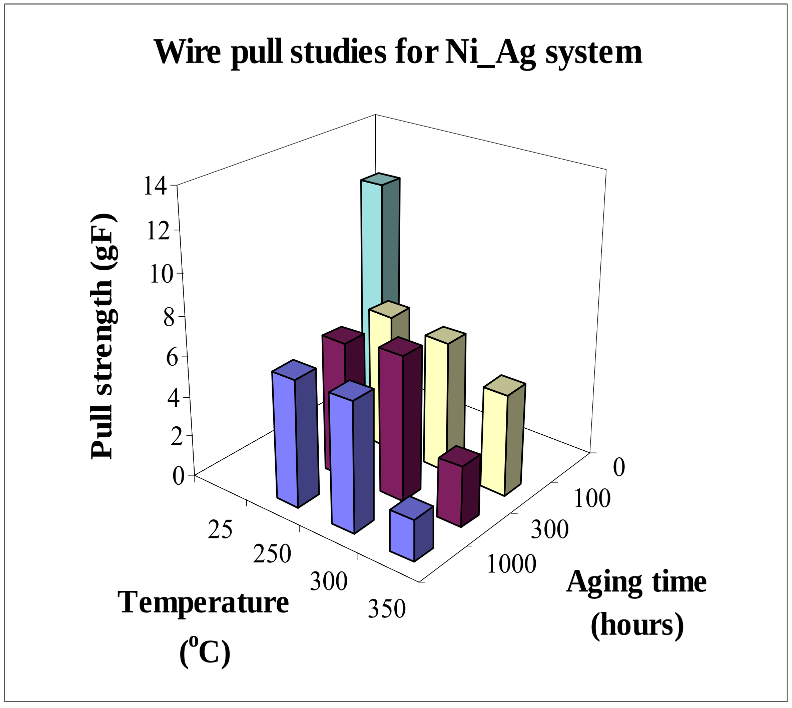
## *Key Features*

- Direct bond copper (DBC) on ceramic ($Al_2O_3$) substrates.
- Silicon dies are soldered to DBC which is soldered to a copper base plate with high lead solder.
- Modules are wire bonded with 125-375 um diameter Al wire.
- The bond wires are bonded such that the height of the first bond pad is significantly lower than that of the second bond pad.
- Silicone gel encapsulant may be used inside the case in the standard module

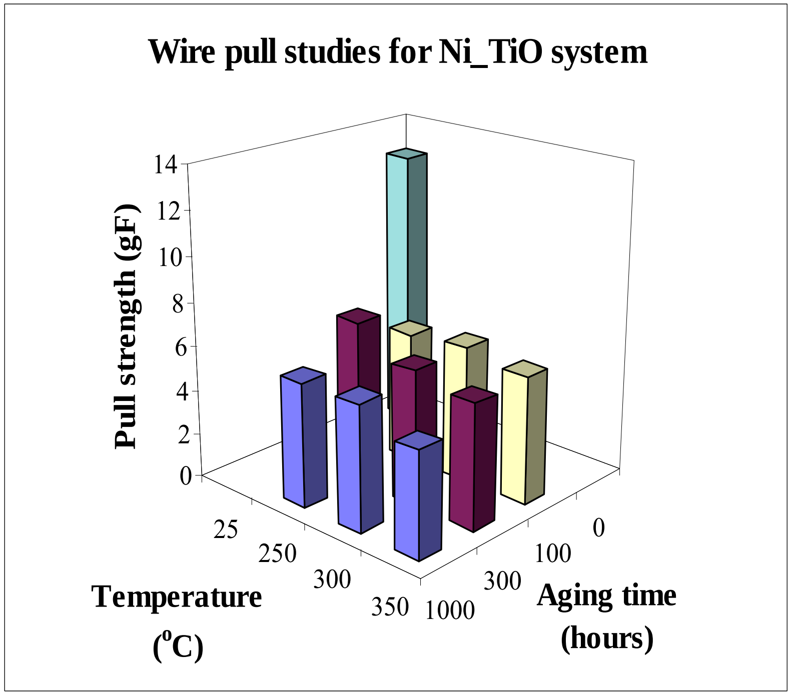


# Pull strength of aged Al-Ni bonds

Al-1%Si wire / Electroless nickel plating on DuPont Invarox 5426 silver thick film on alumina.

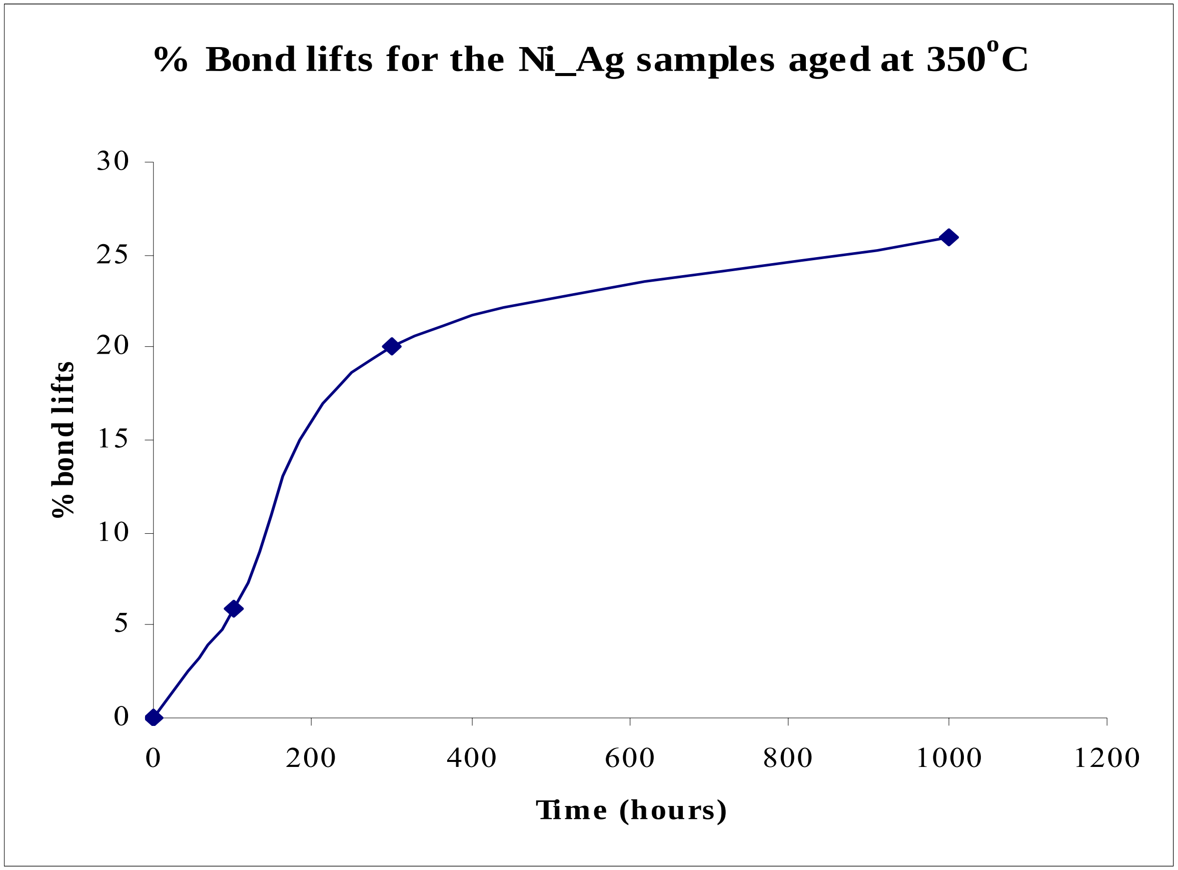



Al-1%Si wire / Sheet nickel active brazed to an alumina substrate using titanium dioxide.




J. Benoit, S. Chin, R. Grzybowski, S. Lin, R. Jain, and **P. McCluskey,** "Wire Bond Metallurgy for High Temperature Electronics" **Proc. of the 4th IEEE Int'l High Temperature Electronics Conference**, Albuquerque, NM, June 14-18, 1998. pp. 109-113.

# Bond lifts observed in Al/Ni-Ag aged at 350°C

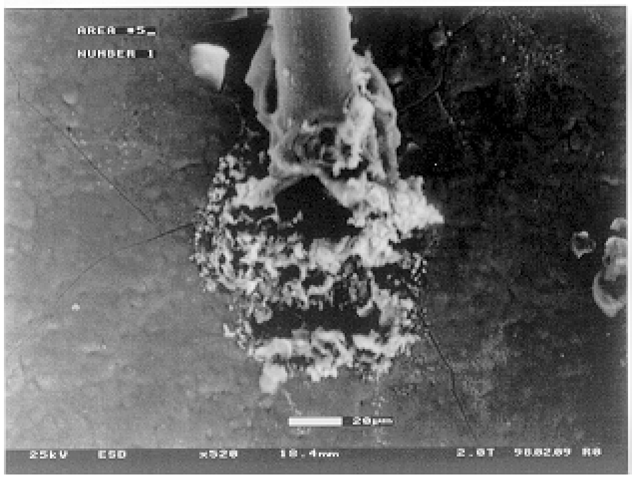



Bond lifts were not observed in the Al/Ni/$TiO_2$ wire bond system.

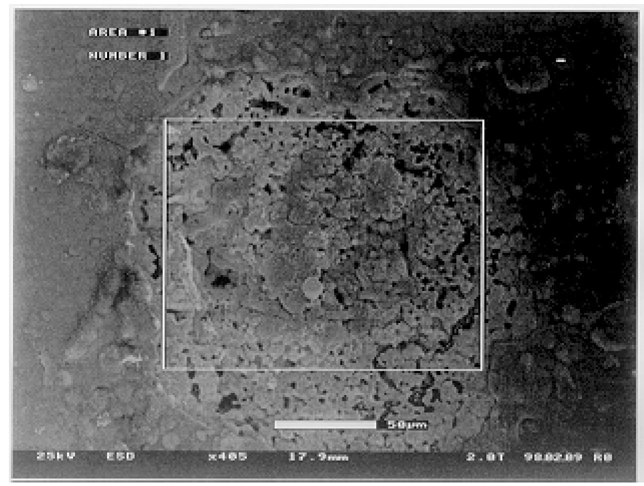
J. Benoit, S. Chin, R. Grzybowski, S. Lin, R. Jain, and **P. McCluskey,** "Wire Bond Metallurgy for High Temperature Electronics" **Proc. of the 4th IEEE Int'l High Temperature Electronics Conference**, Albuquerque, NM, June 14-18, 1998. pp. 109-113.

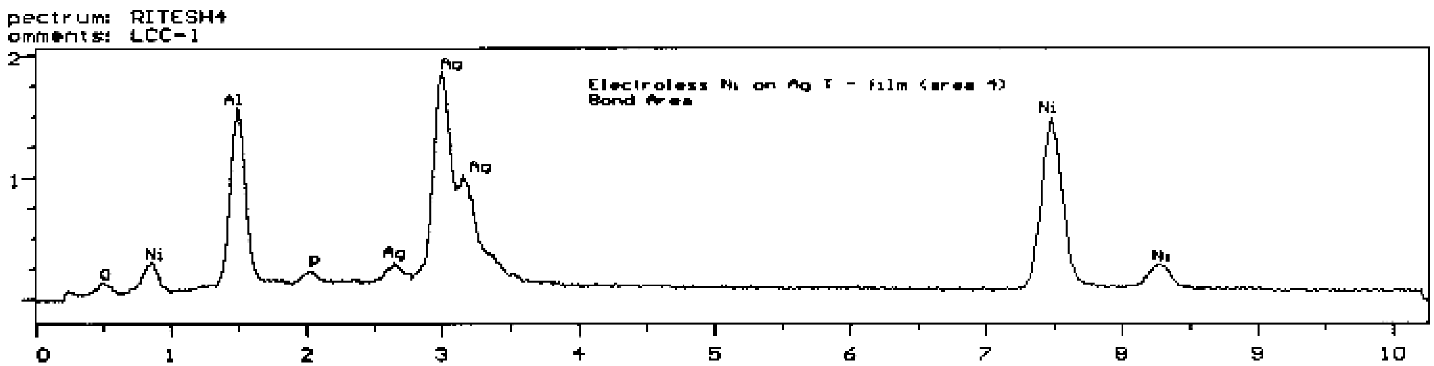
# AlAg intermetallic formed in Al/Ni-Ag system

AlAg intermetallics formed after 1000 hours at 350°C.

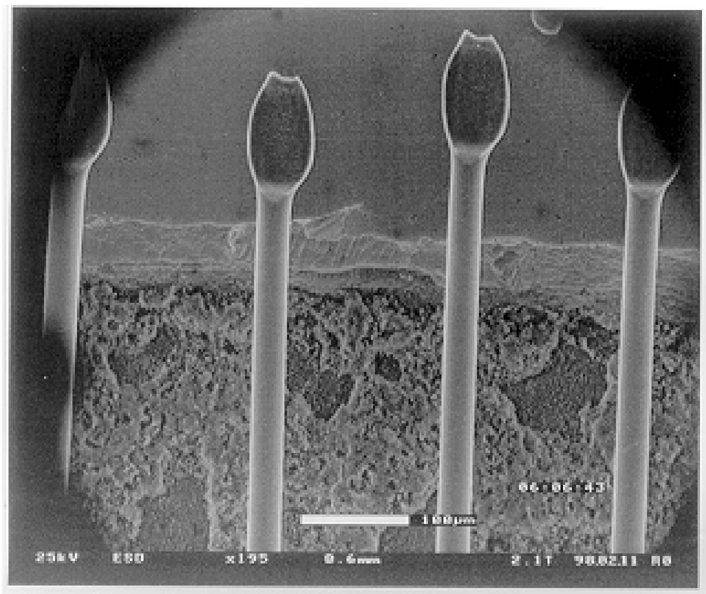



Micrograph showing porosity in the Ni plating revealing Ag.



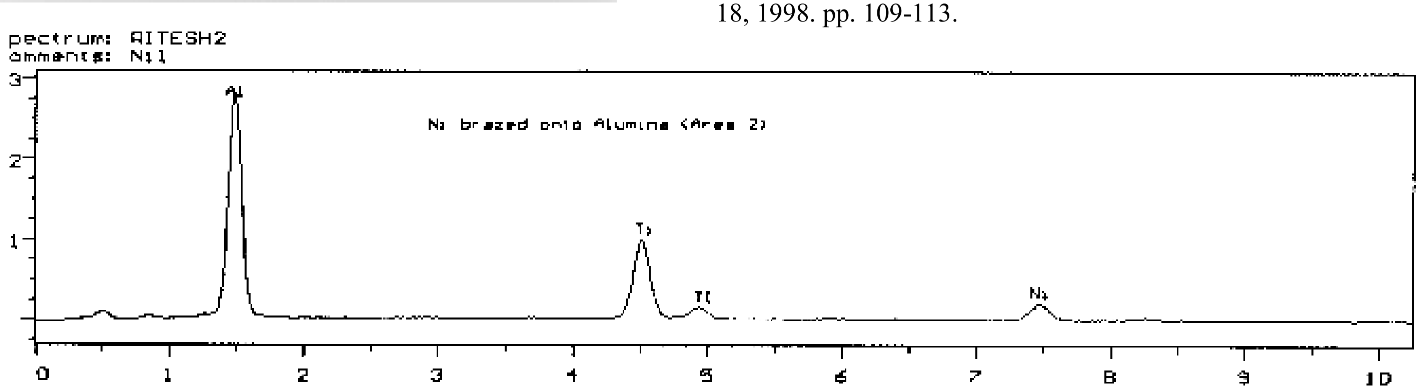



# No degradation in the Al/Ni/$TiO_2$ system




Samples aged at 350°C for 1000 hours indicating no appreciable intermetallic formation at the wire bonds.

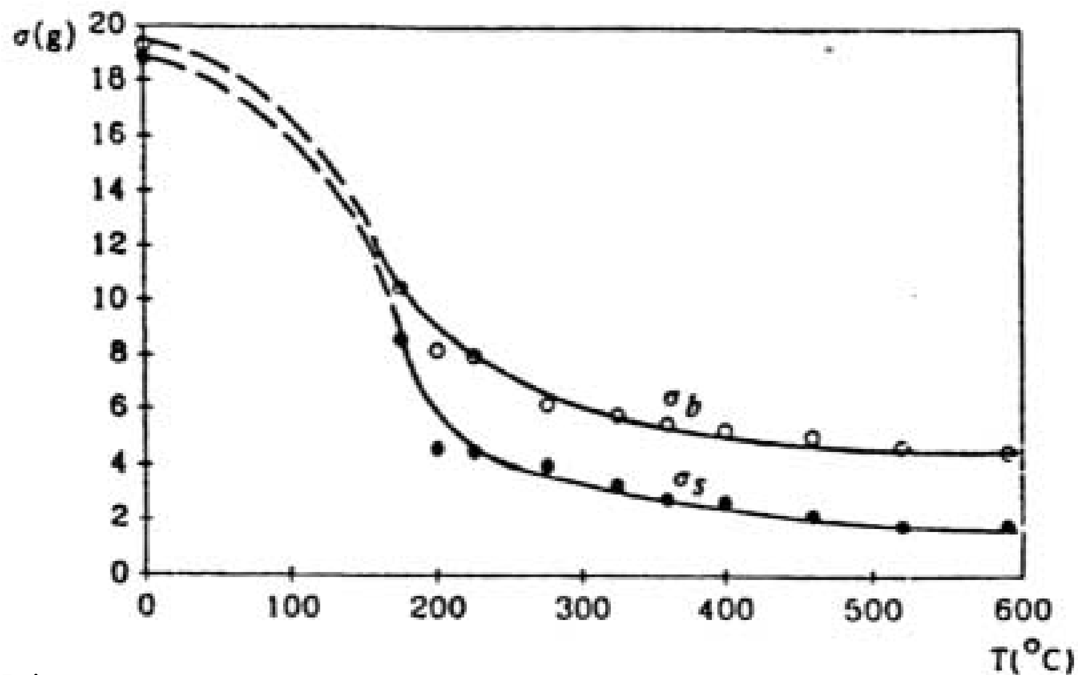
J. Benoit, S. Chin, R. Grzybowski, S. Lin, R. Jain, and **P. McCluskey,** "Wire Bond Metallurgy for High Temperature Electronics" **Proc. of the 4th IEEE Int'l High Temperature Electronics Conference**, Albuquerque, NM, June 14-18, 1998. pp. 109-113.



# Mechanical Strength of Aluminum Wirebonds at High Temperature

37µm Al-1%Si wire

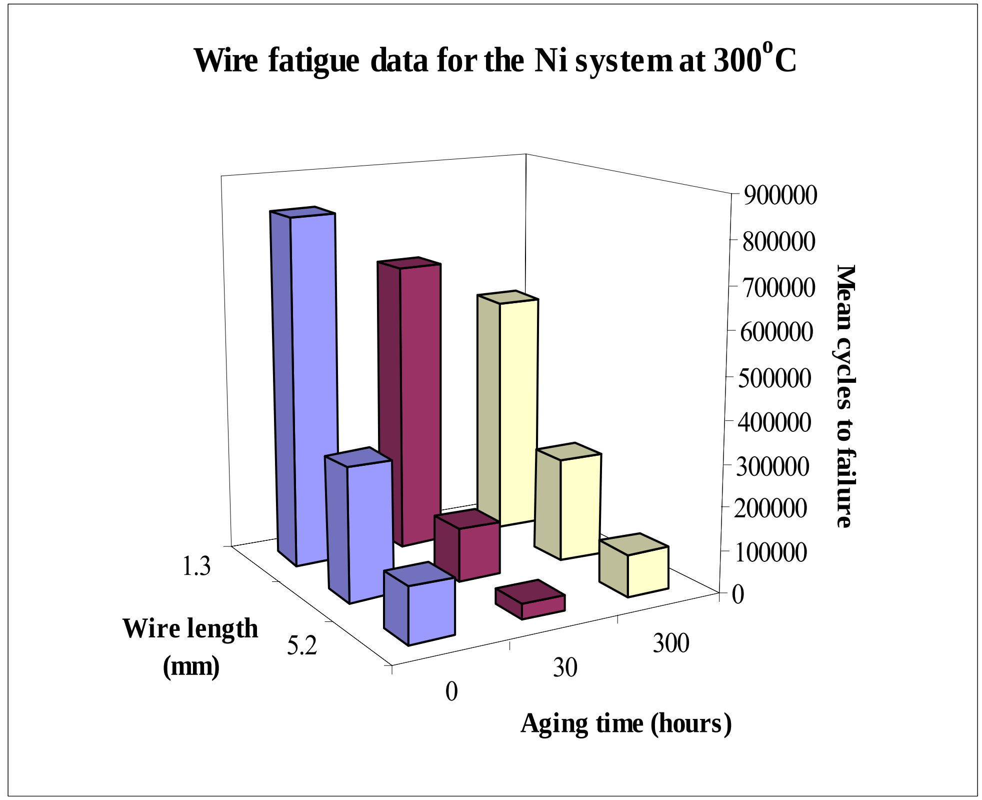
- Yield strength ($\sigma_s$)
- Ultimate strength ($\sigma_b$)




Courtesy of Prof. Wayne Johnson, Auburn Univ.

# Annealing reduces fatigue life

- Longer annealing times decreased fatigue strength in the wires of both systems.
- Comparable results were observed in both systems as the wires used were the same.
- Wires of longer length fail first due to the acute change in angle at the heel of the wire bond.
- No influence of intermetallics on wire fatigue strength.
- 1 mil diameter Al/Al wirebonds fail by the same annealing/fatigue mechanism.

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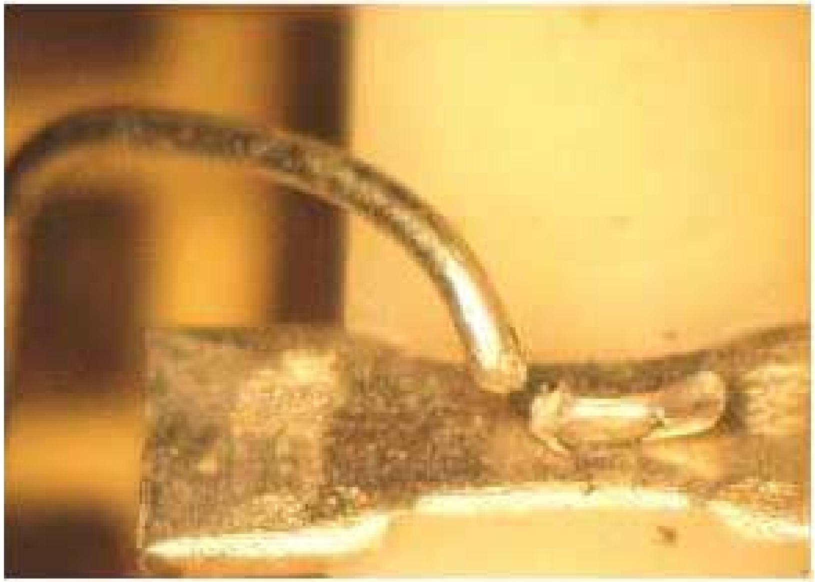
# Wire flexure fatigue

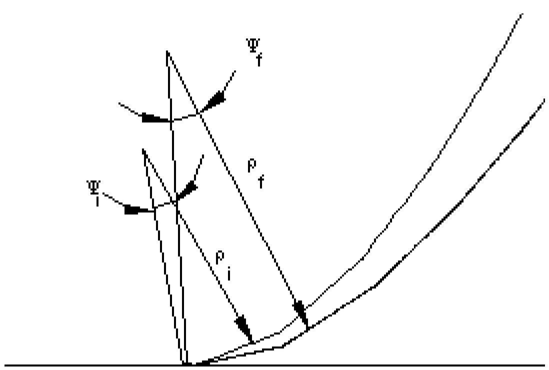


- Power and temperature cycling produce cyclic thermo-mechanical stresses which can lead to wire fatigue failure.
- The stresses arise due to the differential expansion of the wire, the chip, and the substrate causing the wire to flex.
- Flexural stresses concentrate at the heel of the wire on the chip side which experiences greater temperature excursion.
- Leads to intermittents, and open circuits.

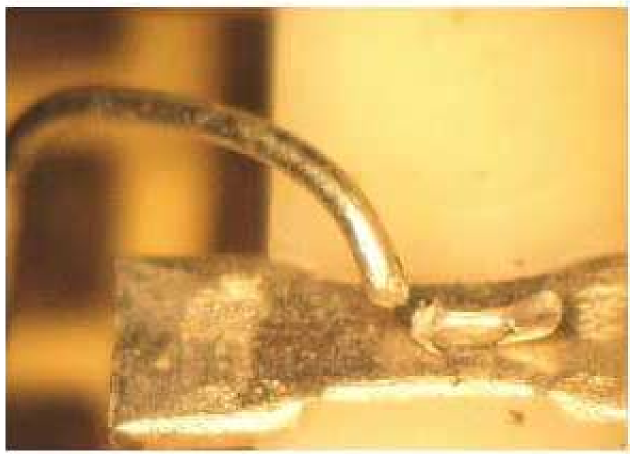
G. Harman, Wire Bonding in Microelectronics: Materials, Processes, and Yield, McGraw-Hill, New York, 1997.

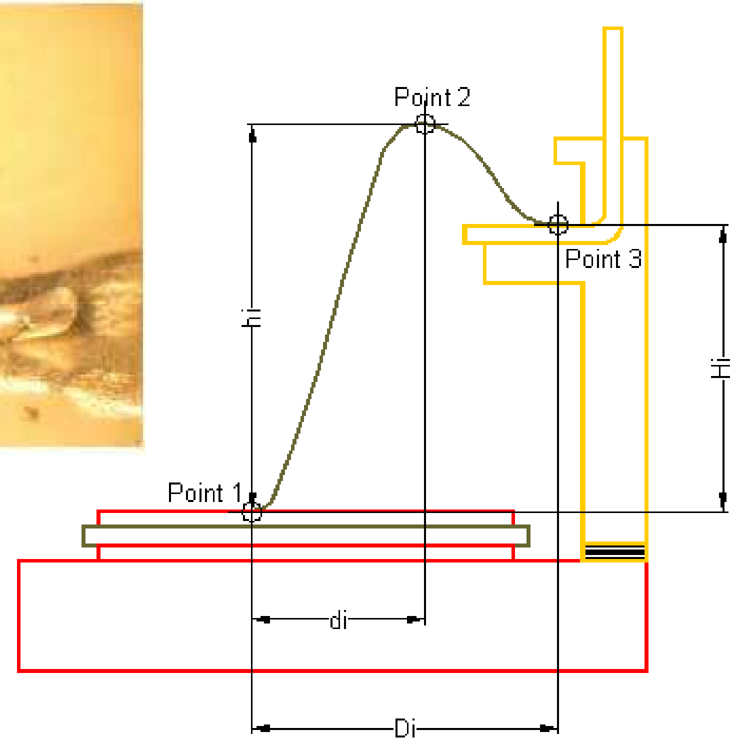
# Wire Flexure Fatigue Modeling

- An analytical model exists to predict the stress/strain at the heel of the bond wire for a wire with bonds that are uneven in height.
- The model takes into account the differential expansion of the wire, the substrate and the frame, using a computer generated fit to the wire geometry for any wire span, length, and downbond height.

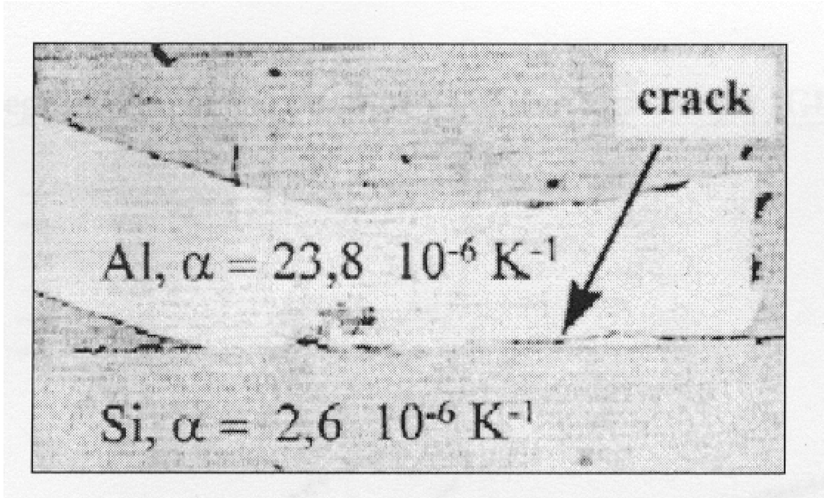


$$\varepsilon = \frac{r(\rho_f - \rho_i)}{\rho_i \rho_f}$$





# Wirebond fatigue

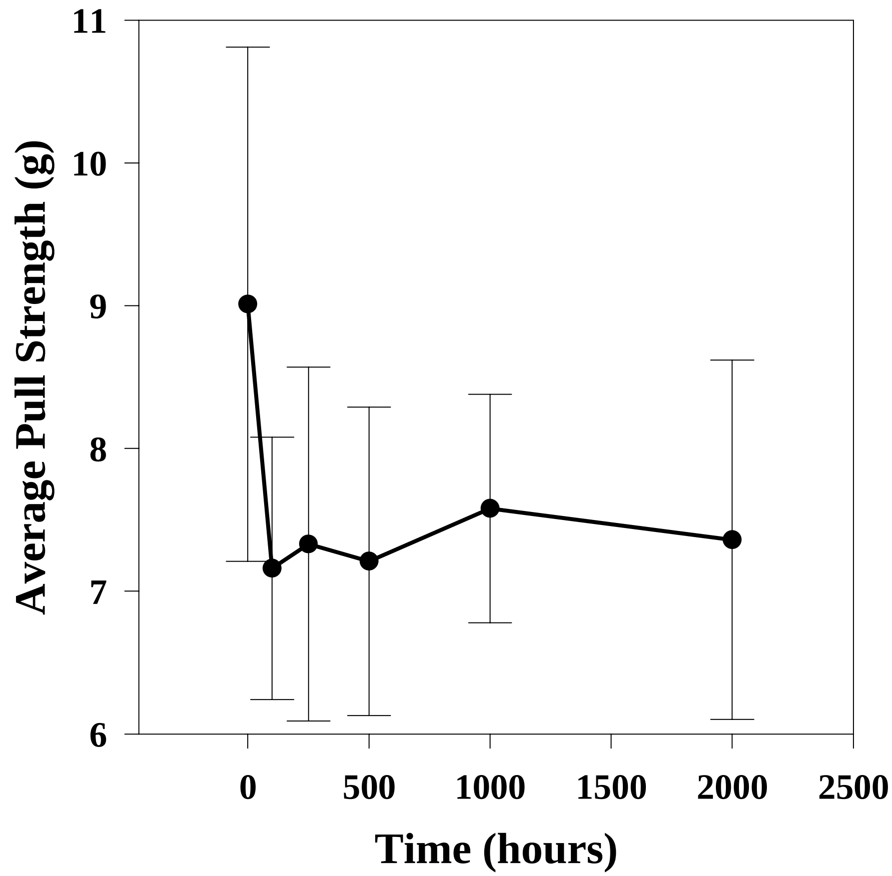



- In 3.3 kV, 1200A IGBT modules, 5-9’s pure Al wires with diameters up to 20 mils (0.5mm) connect the silicon device to the output pins.
- Significant thermomechanical stress is generated in the bonding zone during power/temperature cycling causing wirebond liftoff of emitter contacts
- Can be accelerated by solder joint deterioration

S. Ramminger, Microelectronics Reliability, 2000

# Average Pull Strength of Small Diameter Gold Wire Bonds

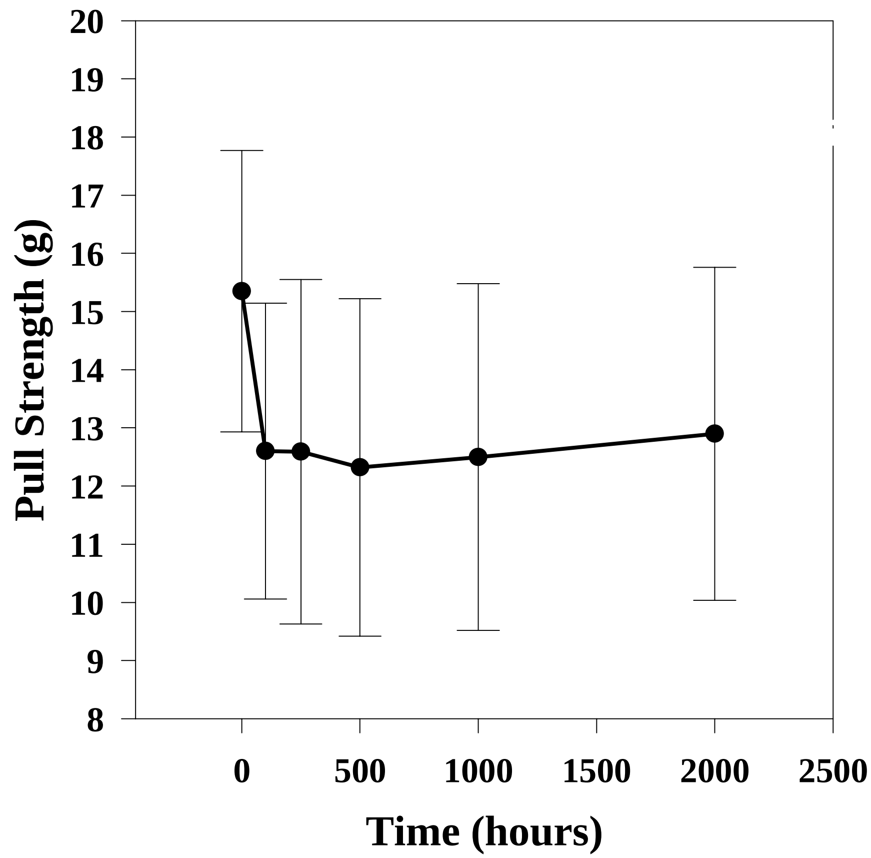
- 25 µm thermosonic gold wire bonds aged at 500ºC for 2000 hrs
- 100 measurements for each data point. Error bars are two standard deviations




Courtesy of Prof. Wayne Johnson, Auburn Univ.

# Average Pull Strength of Small Diameter Platinum Wire Bonds

- 25µm thermosonic platinum wire bonds aged at 500ºC for 2000 hrs
- 100 measurements for each data point. Error bars are two standard deviations




Courtesy of Prof. Wayne Johnson, Auburn Univ.

# Die Attach Materials

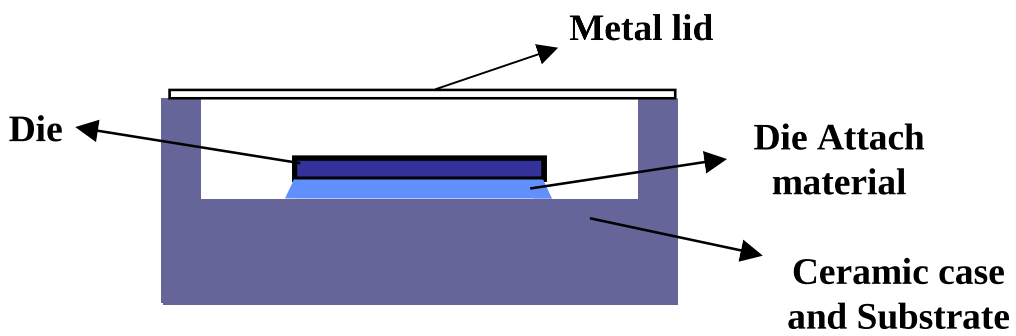
- **Silver-Filled Epoxy Die Attach**
  - Least expensive, widely used in commercial devices
  - Begins to break down at 175°C
- **Polyimide Thermoplastic Die Attach**
  - Able to withstand operating temperatures > 200°C
- **Gold Eutectic Die Attach**
  - Excellent high temperature fatigue and creep resistance
  - Expensive, used for high temperature ceramic packaged devices
- **Solder Die Attach**
  - Pb/Sn (95/5) and Sn/Ag/Sb (65/25/10) are common
  - Used for hybrid devices
- **Silver Glass Die Attach**
  - Excellent fatigue and creep resistance
  - Good thermal stability and conductivity but poor electrical conductivity

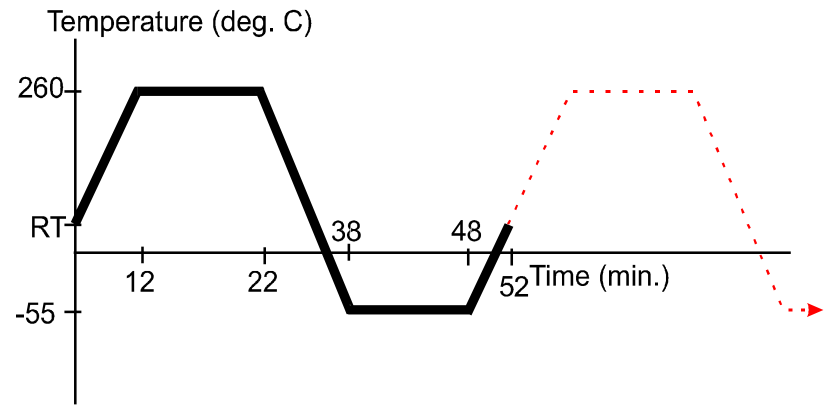
# Die attach materials considered for use at elevated temperatures

DARPA High Temperature Distributed Control Systems Program

| *Material* | *Material Type* | *Filler* | *Max. Potential Operating Temp. ($^oC$)* | *Volume resistivity (ohm-cm)* | *Young's modulus ($10^6$ psi)* |
|---|---|---|---|---|---|
| **JM6100** | **Silver-glass** | **Ag** | **~350** | **2.00E-05** | **3** |
| **QMI** | **Silver-glass** | **Ag** | **~300** | **<15E-06** | **2.19** |
| **71-1** | **polyimide** | **Ag** | **~240** | **1.00E-04** | **1.3** |
| **P-1011** | **polyimide** | **Ag** | **~350** | **1.60E-05** | **0.7** |
| **Staystik501** | **Thermo-plastic film** | **Ag** | **~250** | **<1.00E-04** | **~0.36** |
| **Au-Ge eutectic** | **solder** | **-** | **~340** | | **10.0** |

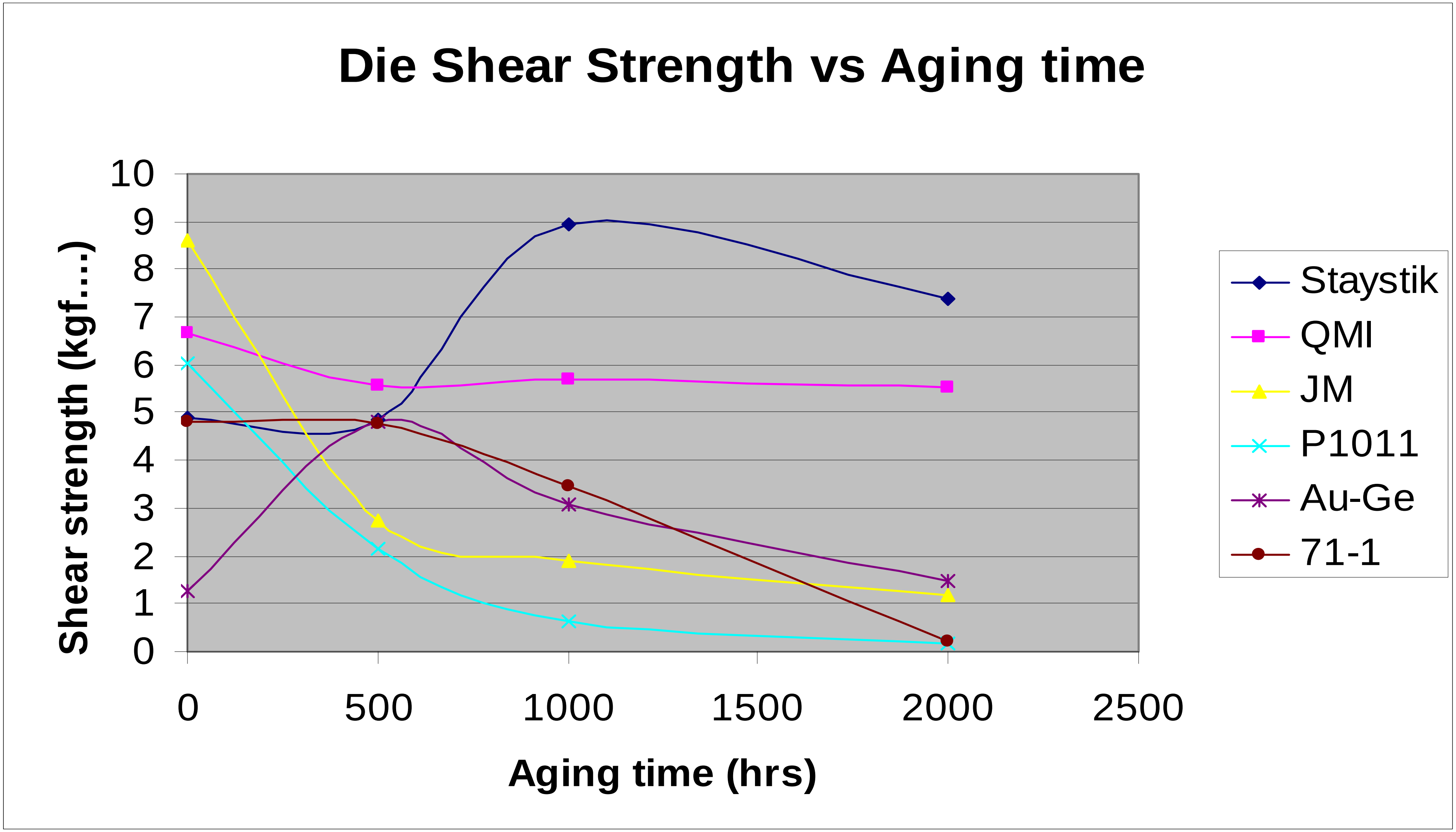
# Die Attach Aging Characterization



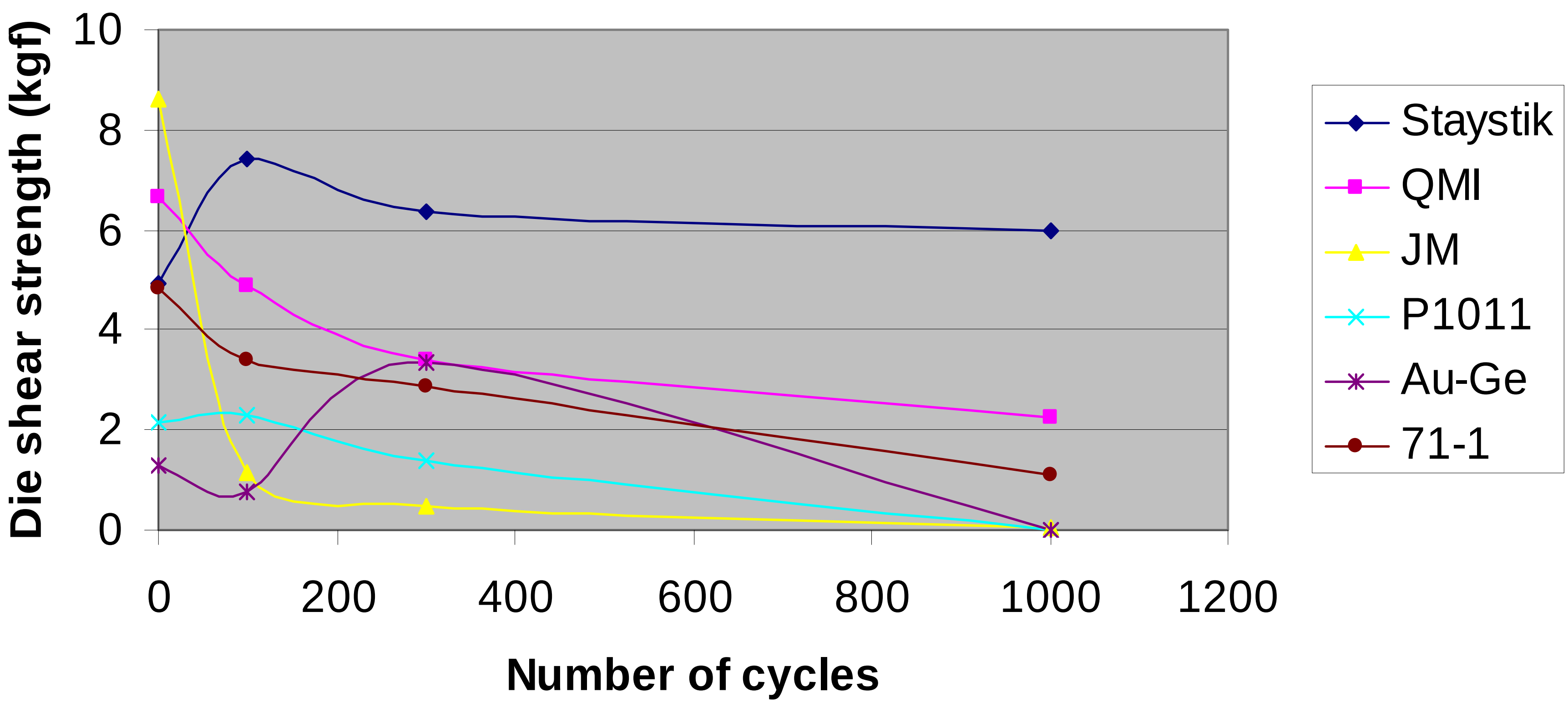




- Test samples with a 40mil x 40mil die bonded on to a ceramic substrate subjected to following tests :

| Control samples | 500 hr aging at 260°C | 1000 hr aging at 260°C | 2000 hr aging at 260°C | 100 cycles of ΔT = 315°C | 300 cycles of ΔT = 315°C | 1000 cycles of ΔT = 315°C |
|---|---|---|---|---|---|---|
| 5 samples per material | 5 samples per material | 5 samples per material | 5 samples per material | 5 samples per material | 5 samples per material | 5 samples per material |

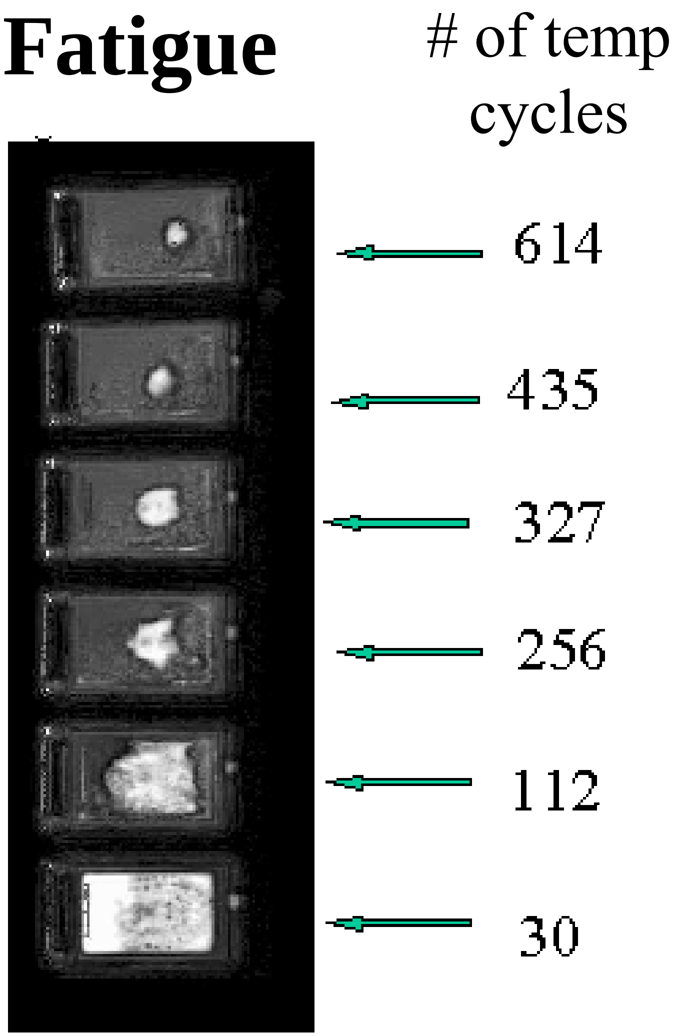

Die Shear Strength vs Aging time
Shear strength (kgf...)
10
9
8
7
6
5
4
3
2
1
0
0
500
1000
1500
2000
2500
Aging time (hrs)
Staystik
QMI
JM
P1011
Au-Ge
71-1

# Die Shear Strength vs Number of Temperature Cycles

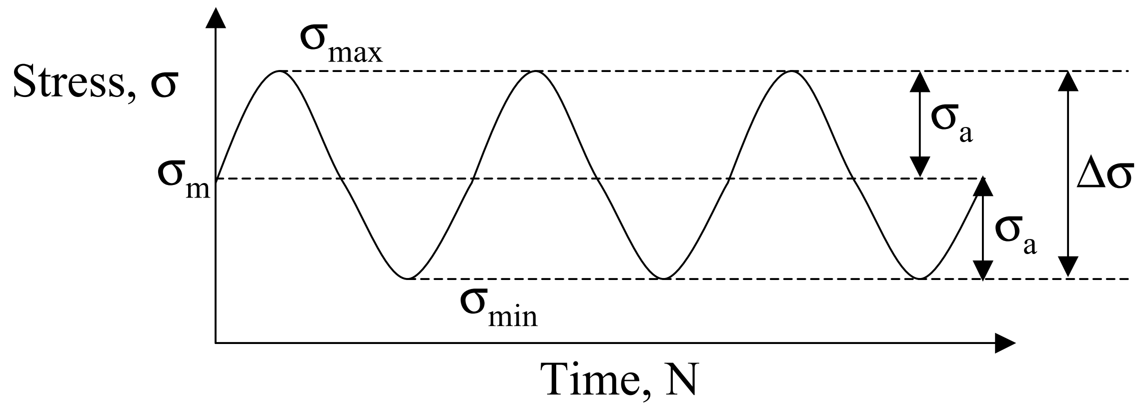


# Large Area Solder Fatigue

- **Failure site:** Die attach
- **Failure mode:** Loss of adhesion between the die and attach leading to open circuit, thermal runaway, mechanical failure.
- **Failure mechanism:** Voids and microcracks initiate at the edge of the die and propagate through the attach layer during temperature cycling due to shear and tensile stresses caused by thermal expansion mismatch between the die and substrate.
- **Environmental/operating stresses:** Power and Temperature cycling



# Mechanical Fatigue Modeling




- High cycle fatigue (uncracked)
  Stresses below the yield strength

$$N_f = C(\Delta\sigma)^{\beta}$$ Basquin's law

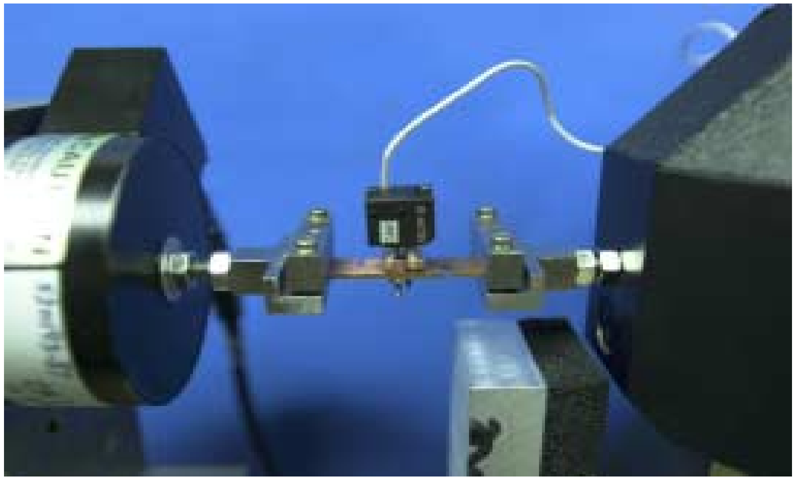
- Low cycle fatigue (uncracked)
  Stresses above the yield strength

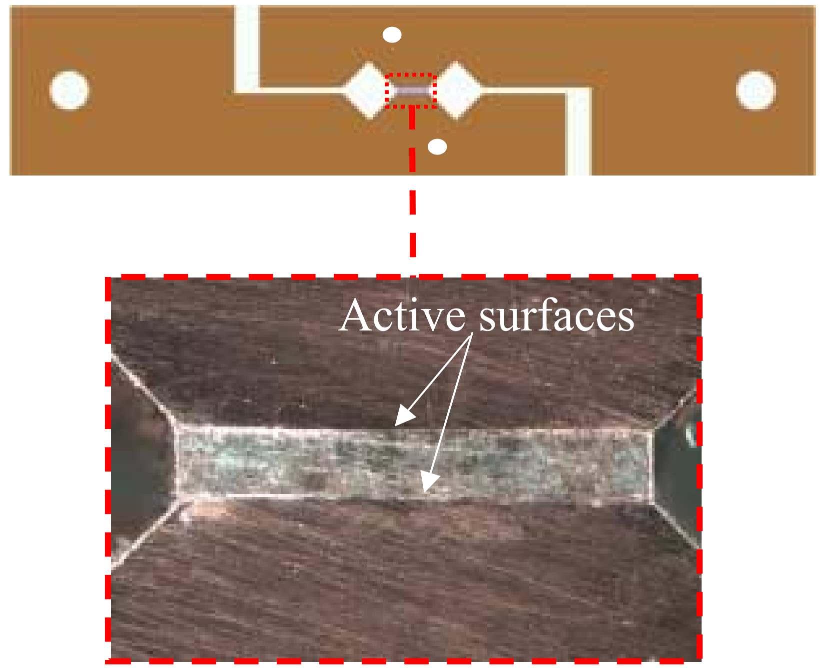
$$N_f = 0.5(\Delta\gamma/2\varepsilon_f)^{1/c}$$ Coffin-Manson and others

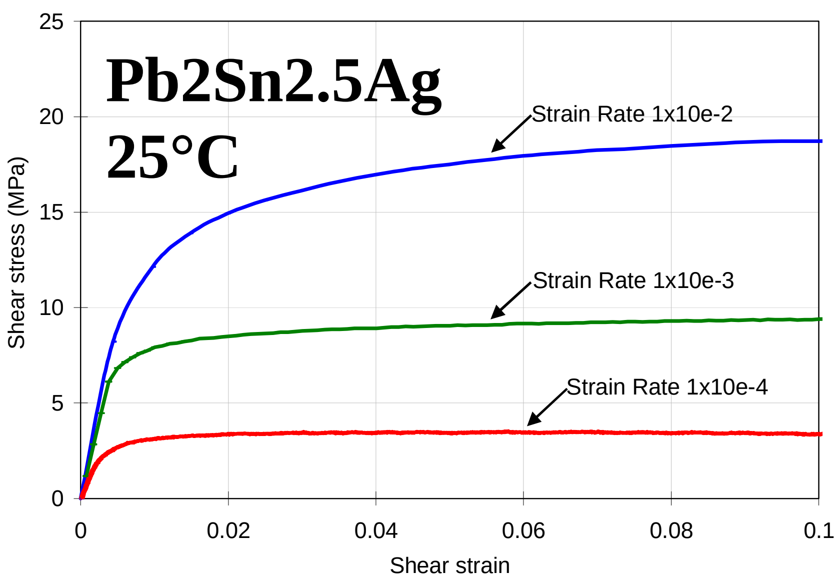
- Fatigue crack growth

$$\frac{da}{dN} = C(\Delta K)^m$$ Paris law

# High Lead Die Attach Property Characterization



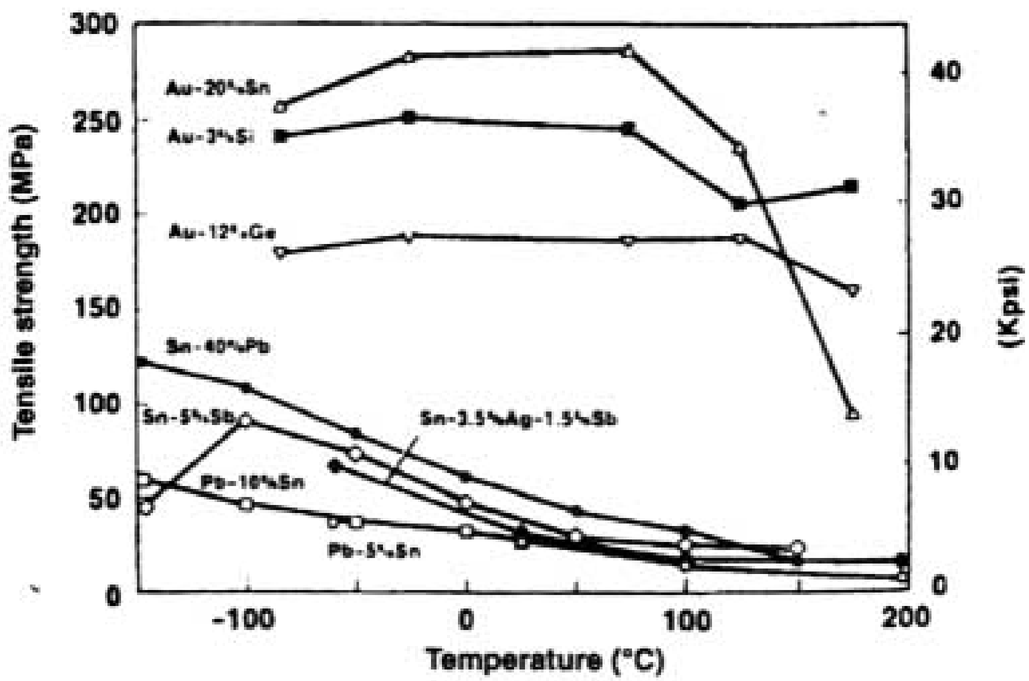



Microfatigue testing is being used to determine the constitutive and fatigue properties of high lead die attach materials

# Standard High Temperature Component Attach Will Not Work at T > 300°C

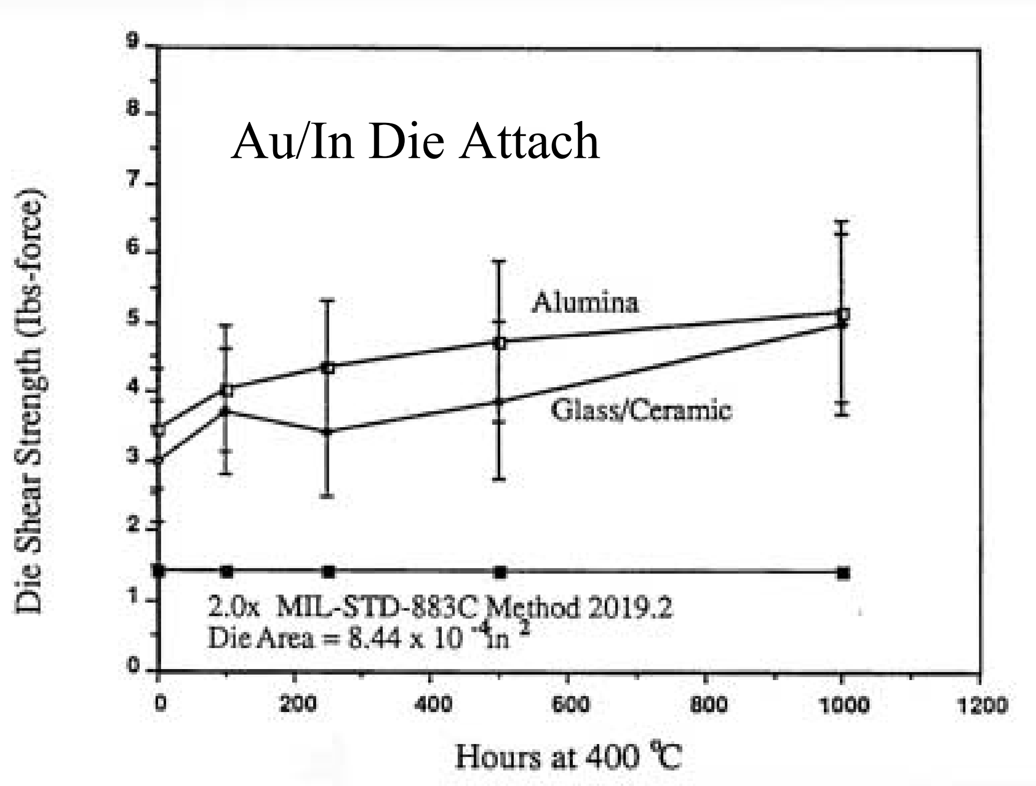
- **Solders**
  - **80Au/20Sn** **280E**
  - **92.5Pb/5Sn/2.5** **280E**
  - **92Pb/5In/3Ag** **300S** **310 L**
  - **95Pb/5Sn** **310S** **314L**
  - **88Au/12Ge** **356E**
  - **96.76Au/3.24Si** **363E**



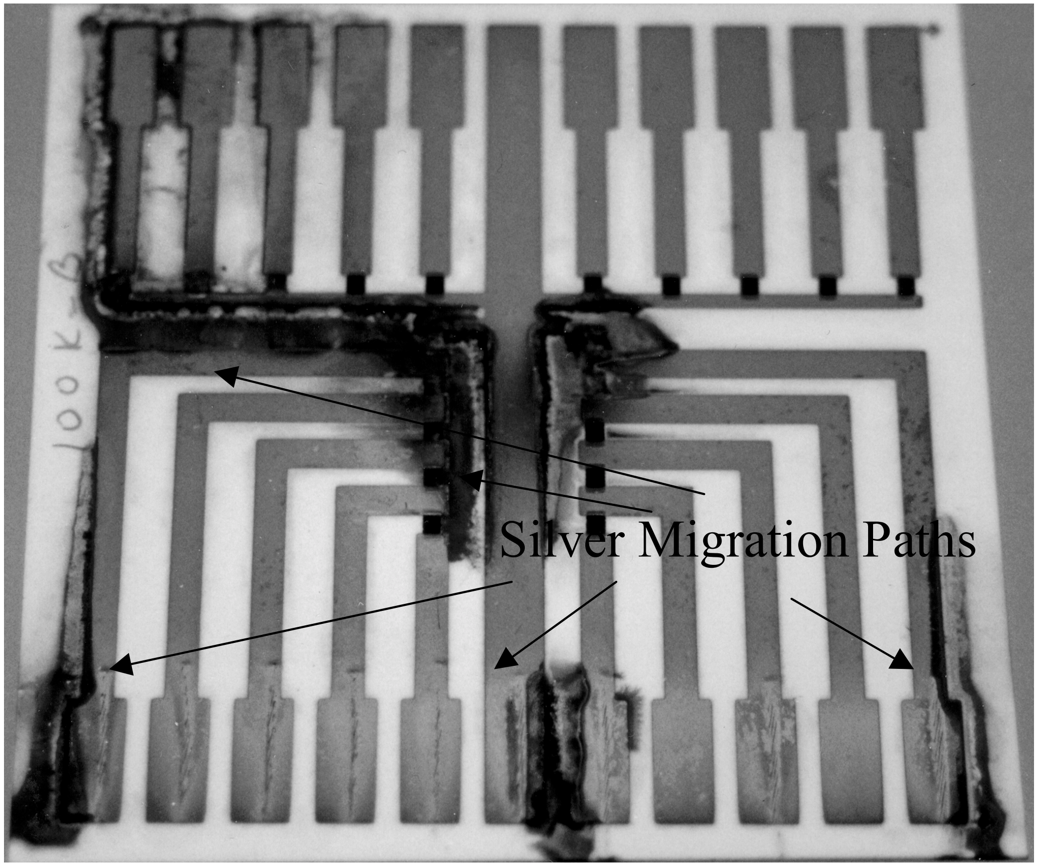
# High Temperature Brazes Required

- **Brazes**
  - **82Au/18In** **451S** **485L**
  - **45Ag/38Au/17Ge** **525E**
  - **72Ag/28Cu** **780E**
  - **82Au/18Ni** **950E**

**Ag will migrate under bias and accelerates with temperature.**

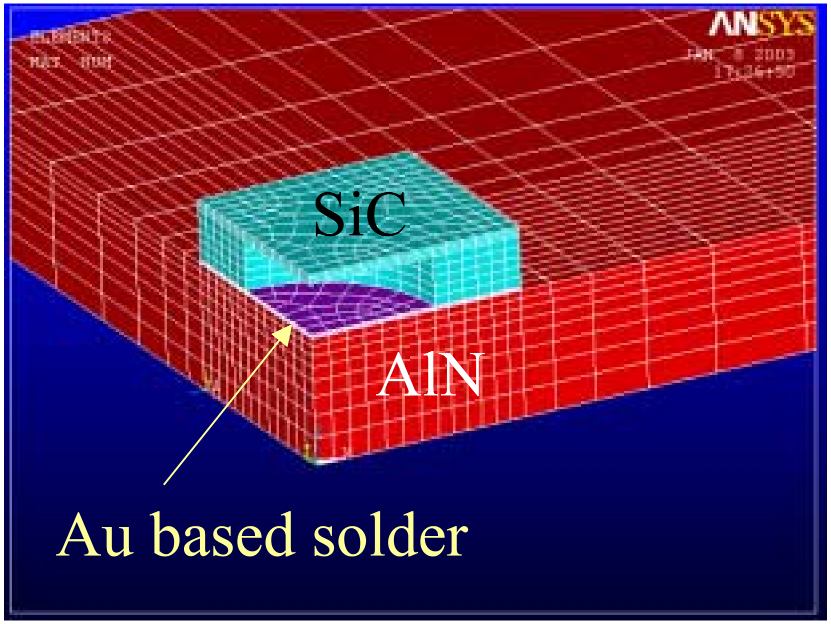


# Silver Migration in PdAg Conductors



# SiC Pressure Sensor Package for 500°C

- Determine the stresses in the SiC, AlN, and die attach as a function of die attach modulus, relaxing temperature, and ΔT.
- Determine the effects of the stress on the mechanical reliability and electrical performance of the SiC pressure sensor for NASA Glenn.



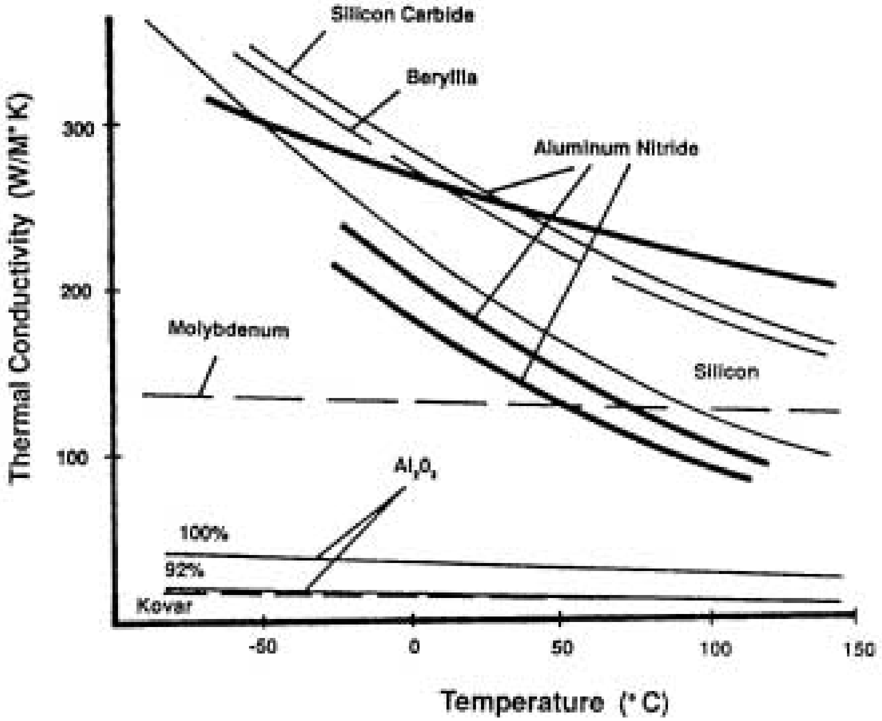

- Possible applications
  - Engine control
  - Lift and attitude control
  - Planetary data collection

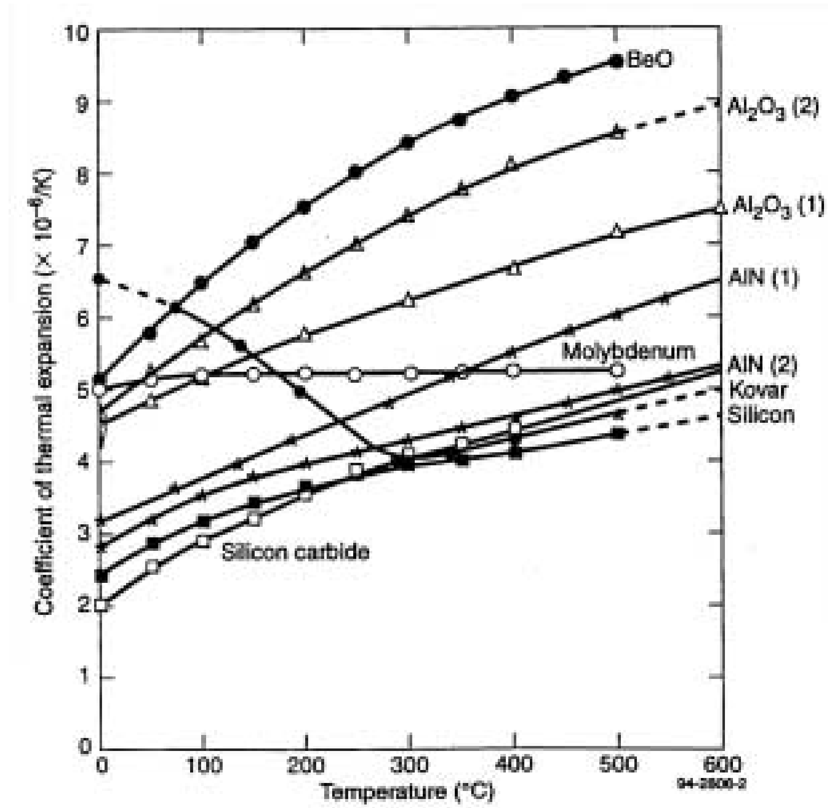
# Substrates

- Alumina
  - Low thermal conductivity
  - High CTE
- Beryllium
  - Limited to 2.9” x 2.3”
  - Higher thermal conductivity
  - High CTE
- Aluminum nitride
  - High thermal conductivity
  - Lower CTE
  - Historically problems with adhesion during wide range thermal cycling
- Direct Bond Copper
- Reactive Brazed Copper
- Plated Copper
  - Thin film adhesion layer
  - Screen printed refractory metal

# Substrates

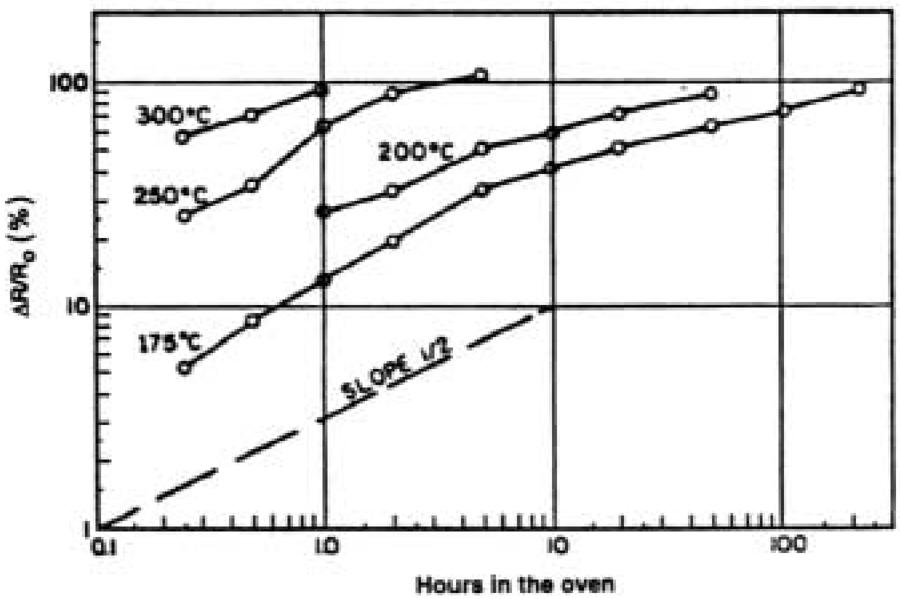
Need to balance thermal conductivity and coefficient of thermal expansion.



# Degradation of Metallization

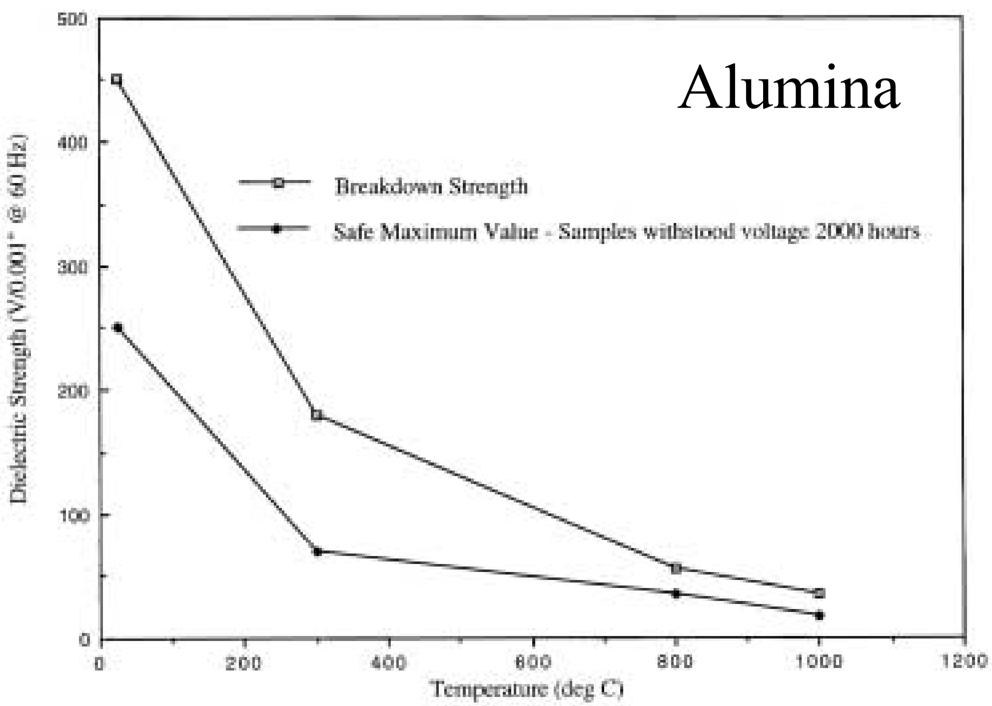
- **Base Metal Diffusion**
  - **Ti/Pd/Au thin film**
  - **250°C**
- **Loss of Conductivity**
  - **Ti/Pd/Au thin film**
  - **% ΔR**



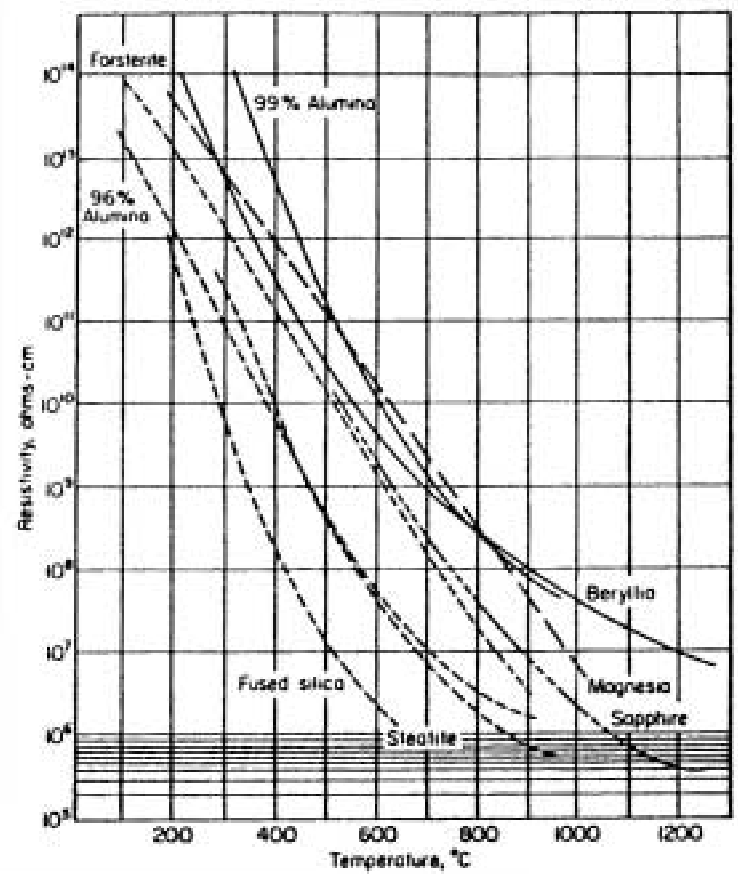

Courtesy of Prof. Wayne Johnson, Auburn Univ.

# Electrical Properties

## Breakdown Strength

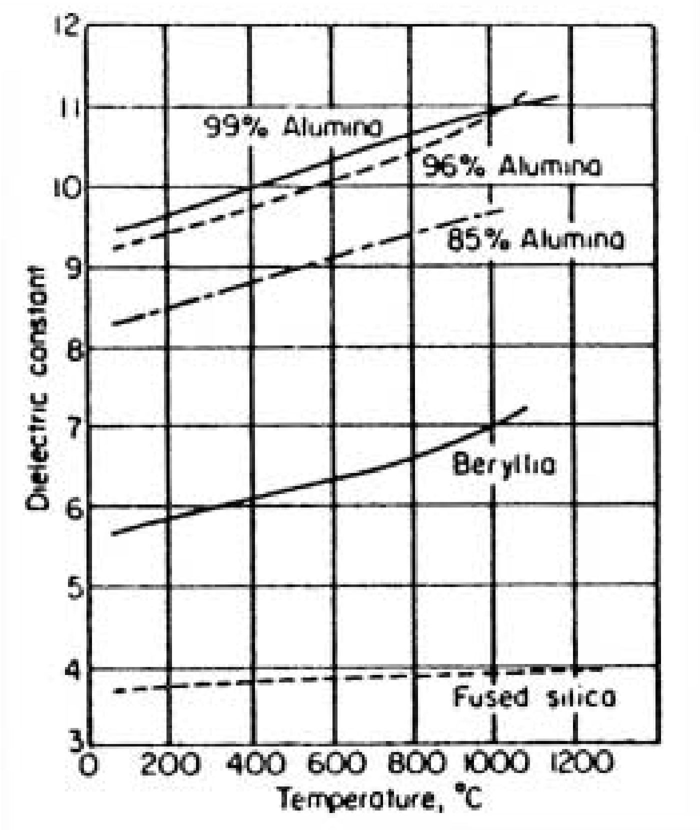



## Volume Resistivity

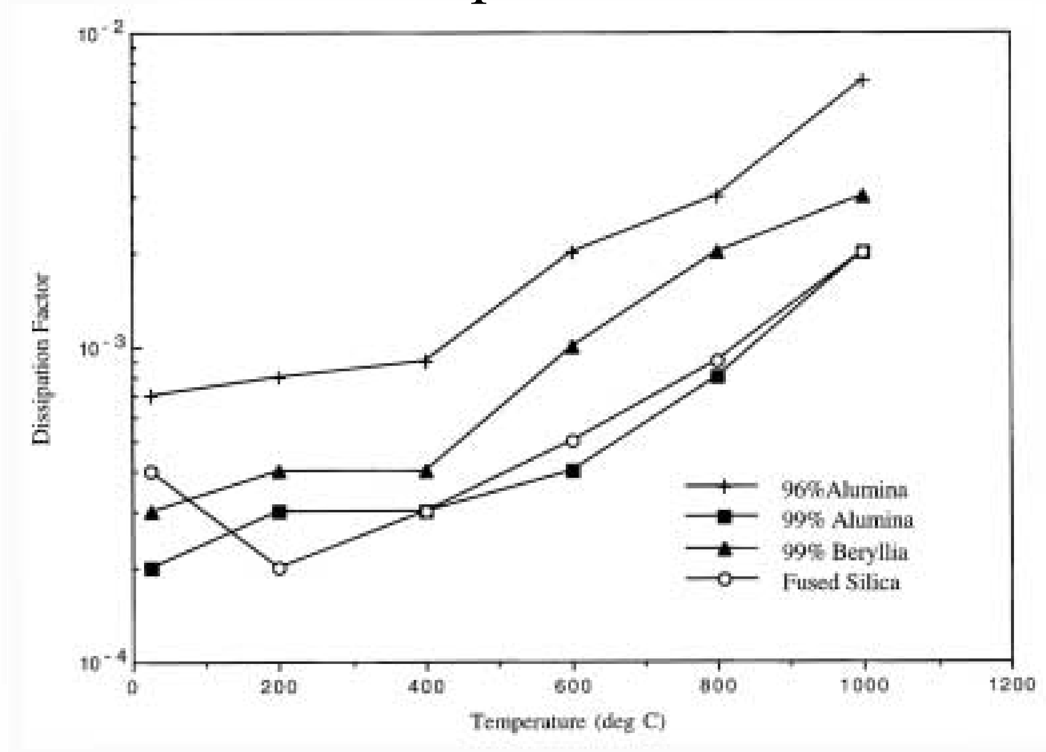


# Electrical Properties

## Dielectric Constant




## Dissipation Factor



# Substrates - Thick Film Hybrids

- **Base Substrate**
  - **$Al_2O_3$: 800°C**
  - **AlN: >500°C**
  - **BeO: 800°C**
- **Metallization**
  - **Au, Au-Pt, Au-Pd: 500°C**
- **Dielectrics**
  - **Glass/Ceramic: 200°C - 500°C**
- **Resistors**
  - **Metal Oxides/Glass: 500°C**
  - **Heraeus Cermalloy 900 Series**

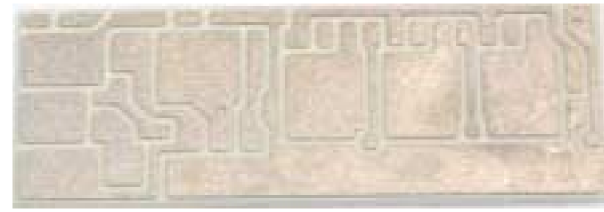
# Substrates - Thin Film Hybrids

- **Base Substrate**
  - **$Al_2O_3$: 800°C**
  - **AlN: >500°C**
  - **BeO: 800°C**
- **Metallization**
  - **NiCr/Ni/Au: 250°C**
  - **Ti/Pd/Au: 200°C**
  - **Cr/Cu/Ni/Au: 250°C**
- **Resistors**
  - **NiCr: 200°C**
  - **$Ta_2N$: 200°C**

# Substrates - Cofired

- Cofired Ceramic: 500$^{o}$C
  - $Al_2O_3$, AlN, BeO
  - W, Mo, Ni/Au Plated
- Glass-Ceramics: 500$^{o}$C
  - Glass/Ceramic, Re-crystallizing Glass
  - Au, Au-Pt, Au-Pd
  - Metal Oxide/Glass Resistors

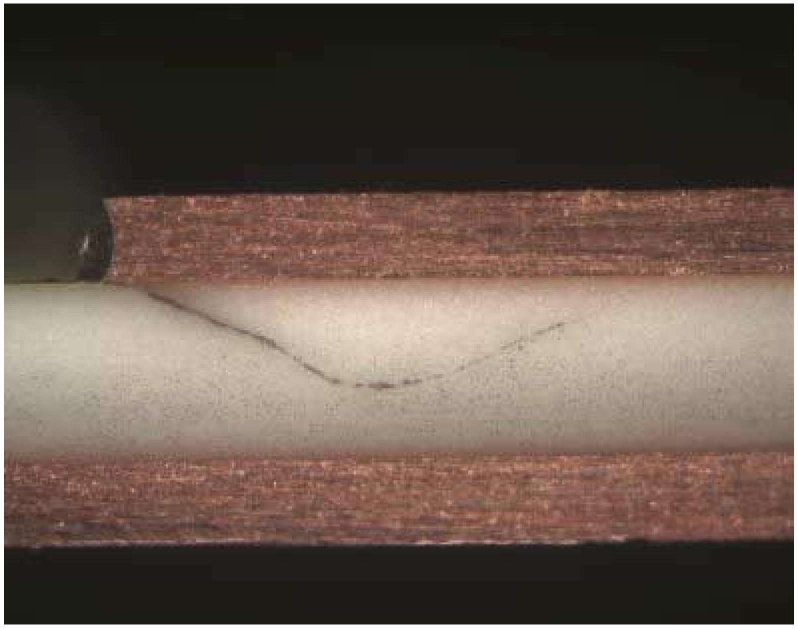
# Advantages of DBC



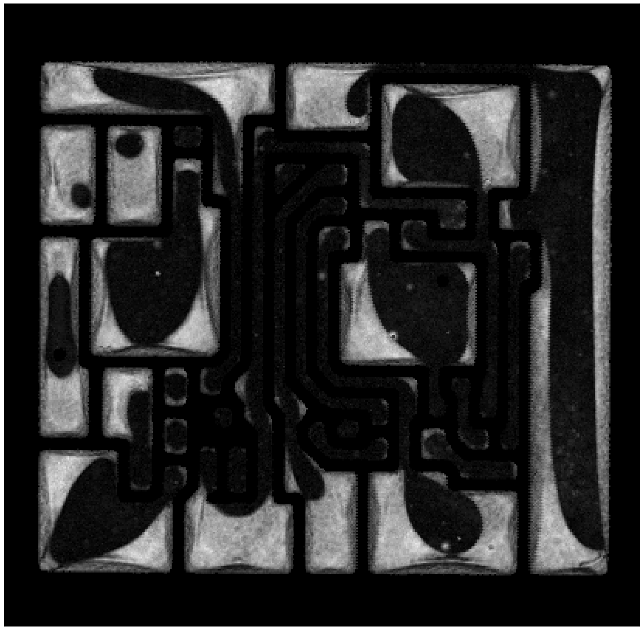
- Since the mid-1980s, direct bond copper has become the preferred substrate for chip-on-board power electronic assemblies because of its excellent price/performance ratio and reliability.
- DBC consists of a ceramic insulator, usually $Al_2O_3$ (alumina) but sometimes AlN (aluminum nitride), onto which 0.2-0.3 mm thick, high purity, solid copper is bonded in a 1075°C melting/diffusion process conducted in a controlled atmosphere.
- The good thermal conductivity of $Al_2O_3$ (24 W/mK) and the excellent conductivity of AlN (180W/mK) combined with the high thermal capacity and thermal spreading capability of thick, high purity copper makes DBC an excellent choice for high power dissipating circuits.
- The CTE of $Al_2O_3$ (7.2 ppm/K) and AlN (4.9 ppm/K) closely match that of silicon (2.6 ppm/K), minimizing mechanical stress in the bare die and attach.
- Alternatives to DBC, such as printed wiring boards, copper thick film ceramic substrates, and insulated metal substrates are usually restricted to power levels below the ones possible with DBC.

*Curamic ® www.curamik.com*

# DBC failure – Crack path



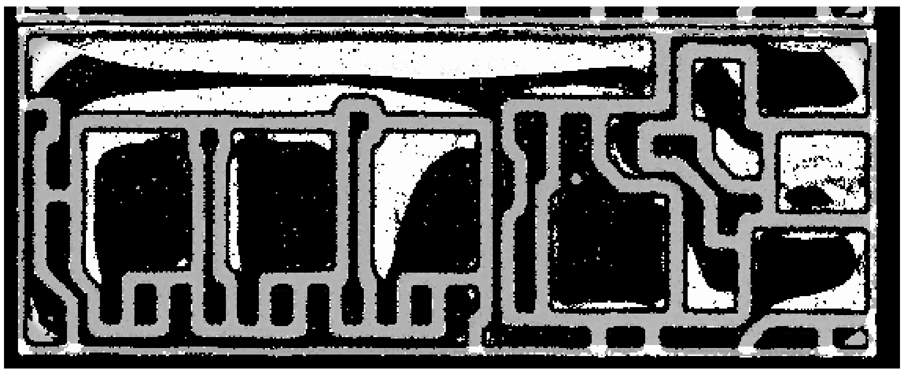
Crack visible in DBC cut using low speed saw



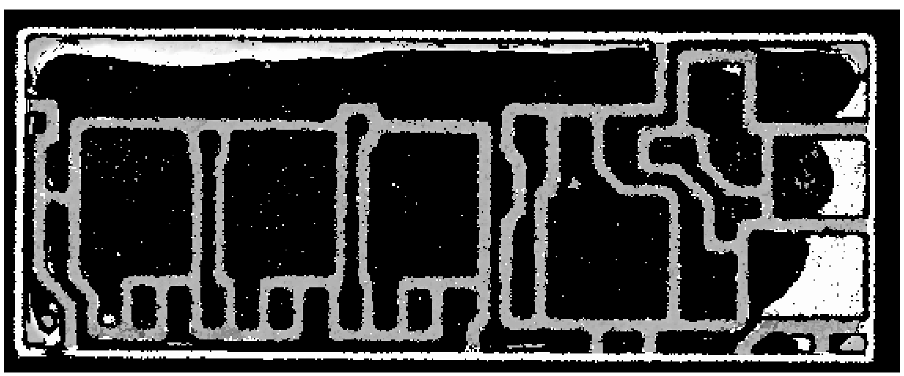
C-SAM

Acoustic impedance of Cu and Alumina are almost equal. Therefore there will be no reflected energy when the bond is good. Cracks thus give good contrast in C-SAM.

# Less cracking observed on mounted samples



DBC not bonded during thermal cycling.



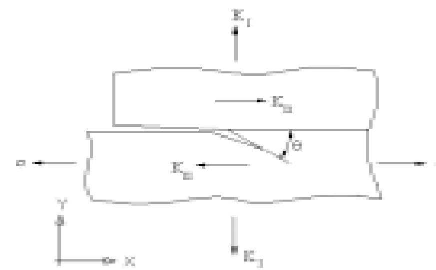
DBC solder bonded to a 4mm Cu heat sink during thermal cycling.

*PCIM 2001: Failure Analysis on Direct Bonded Copper Substrates.*

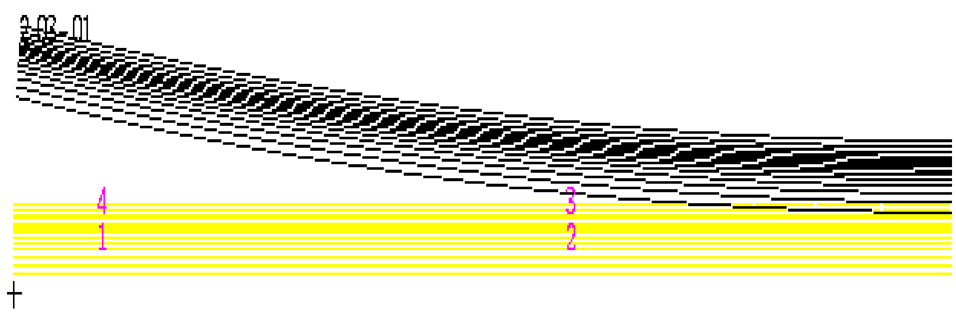
The interface crack grows at a shallow angle under a mixed mode I and mode II loading condition.

Analytical model which gives the number of cycles to failure is developed based on Paris law.

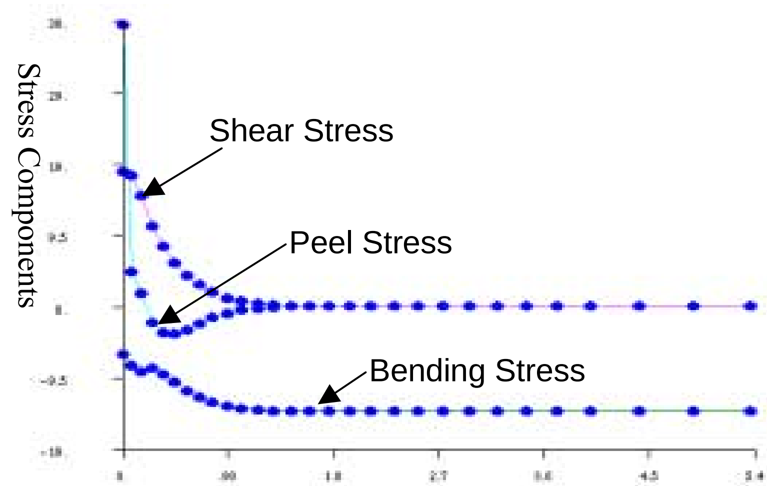
$$\frac{da}{dN} = A(\Delta K)^n \quad \text{where } \Delta K=[K_I^2+K_{II}^2]^{0.5}$$



Mixed mode fracture in DBC



Deformed view of the DBC on thermal cycling




Stresses at the interface of DBC

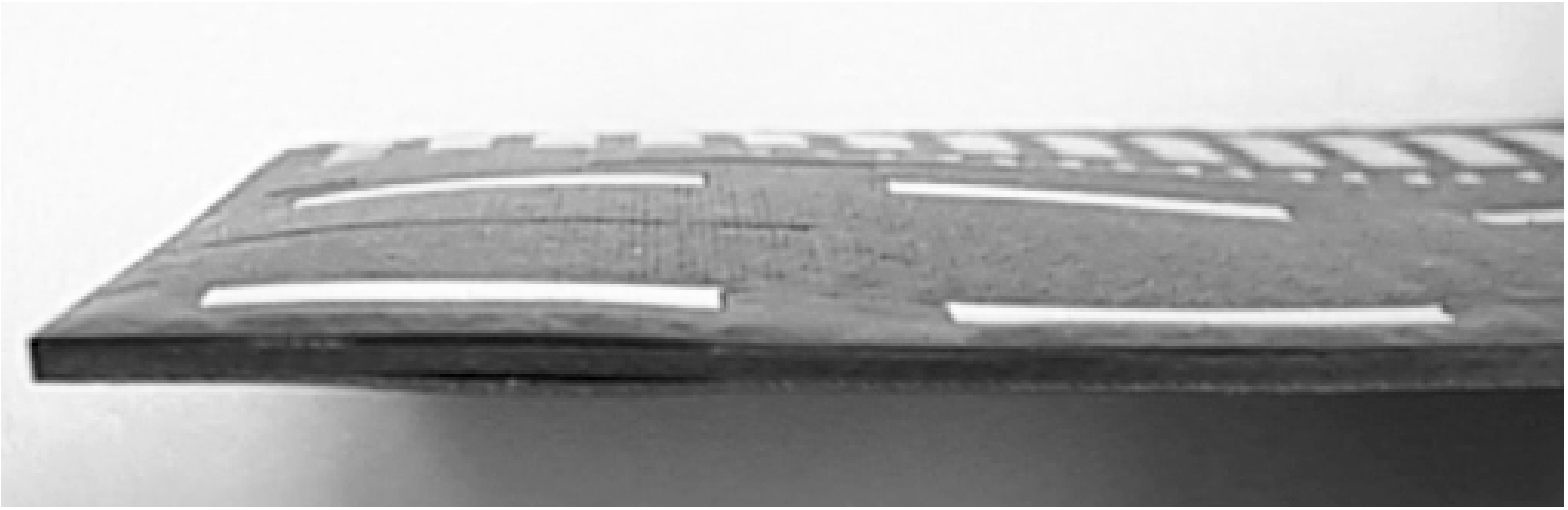
# Encapsulation

- Metal
  - Kovar with glass feedthroughs: 400$^{o}$C
  - Kovar with ceramic feedthroughs: 500$^{o}$C
  - Copper (Cu-sil): 300$^{o}$C
- Ceramic
  - $Al_2O_3$, AlN
- Sealing
  - Resistance Welding
    - Seal Ring Required for Ceramic Package
  - Brazing
  - Glass Seal (Ceramic packages)

# Availability of High Temperature PWBs

| Material | $T_g$ (°C) | Dielectric Constant | CTE-Z ppm°C | CTE-X ppm°C | CTE-Y ppm°C |
|---|---|---|---|---|---|
| FR4<br>Tetrafunctional | 135<br>142 | 4.5 | 60 | 15 | 15 |
| FR4 Tetra 11 #370 | 175 | 4.4 | 60 | 15 | 15 |
| Fr4 Tetra 11 Plus #370-G | 180 | 3.9 | 45 | 14 | 14 |
| Getek | 180 | 3.9 | 50 | 13 | 13 |
| B-T | 180 | 4.1 | 50 | 13 | 13 |
| Thermount | 220 | 4.1 | 85 | 8.5 | 8.5 |
| Polyimide Blend | 225 | 4.3 | 70 | 13 | 13 |
| Cyanate Ester E-Glass | 250 | 3.8 | 55 | 12 | 12 |
| Cyanate Ester S-Glass | 250 | 3.6 | 50 | 9 | 9 |
| Polyimide 85NT | 250 | 3.9 | 100 | 6-9 | 6-9 |
| Polyimide E-Glass | 260 | 4.3 | 70 | 13 | 13 |

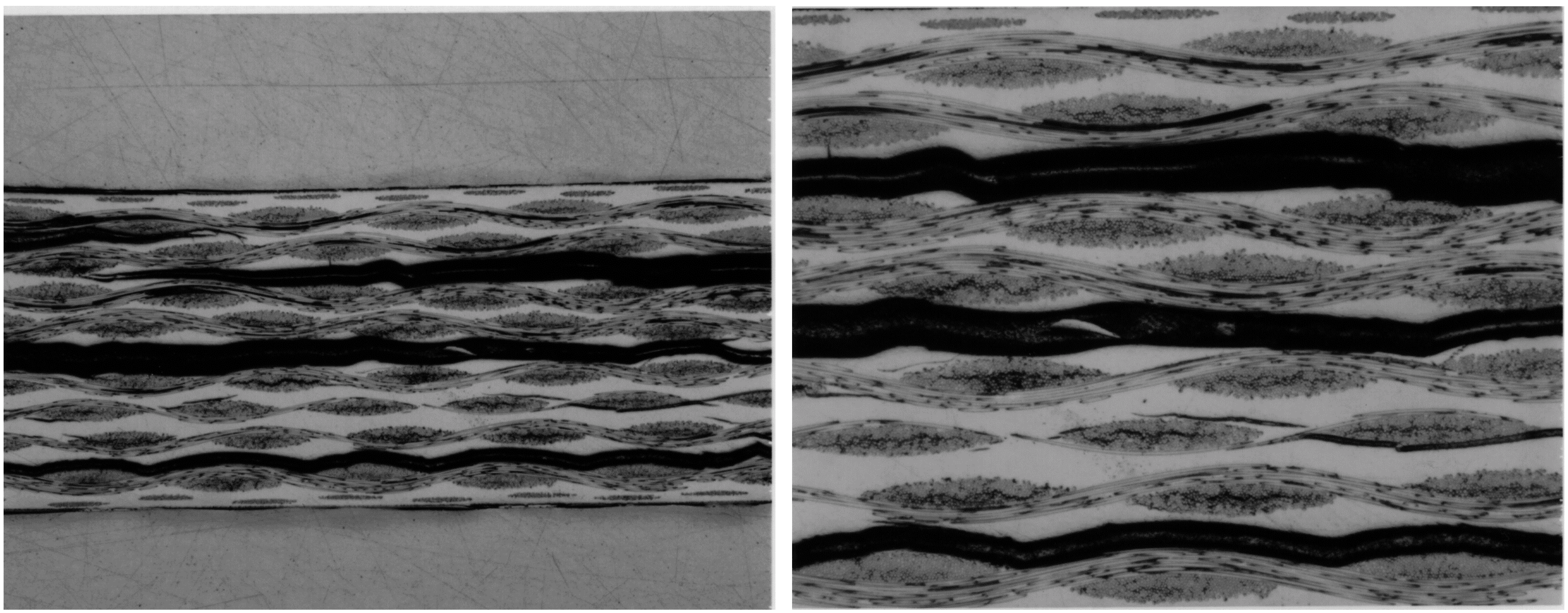
# Cyanate Ester at 250$^{o}$C



## Delamination of copper above Tg

Courtesy of Prof. Wayne Johnson, Auburn Univ.

# Nelco N7000 PWB Following Solder Reflow Cycle



Courtesy of Dr. Richard Grzybowski and United Technologies

# Criteria for High-Temperature Solders

- Good wettability
- Narrow melting temperature range
- High shear strength
- High fatigue resistance
- Corrosion/oxidation (dross formation) resistance
- Melting temperature higher than 200$^{o}$ C
- Compatibility with other components, systems, and processes
- High creep resistance at elevated temperatures
- Non-toxic (lead free preferred)
- Low cost

# Solder Materials

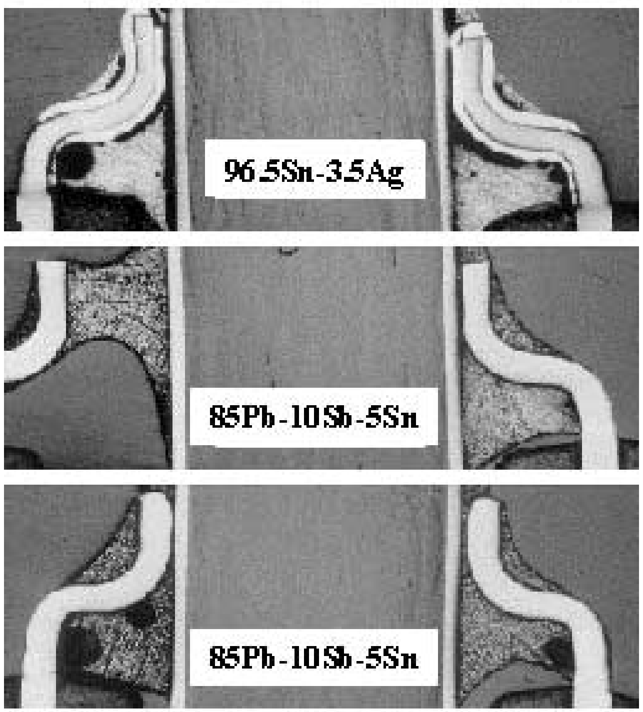
| Solder | Solidus | Liquidus | Solder | Solidus | Liquidus |
|---|---|---|---|---|---|
| Sn62Pb36Ag2 | 179°C | 179°C | **Sn95Sb5** | **235°C** | **240°C** |
| Sn63Pb37 | 183°C | 183°C | **Pb75In25** | **250°C** | **265°C** |
| Sn60Pb40 | 183°C | 191°C | Sn95Cu3Sb1Ag1 | -------- | 256°C |
| Pb60In40 | 195°C | 225°C | **Pb88Sn10Ag2** | **268°C** | **290°C** |
| Sn92Ag3Bi5 | 210°C | -------- | **Pb90Sn10** | **268°C** | **-------** |
| Sn96Cu1Sb1Ag2 | 210°C | 217°C | Bi95Sb5 | 275°C | 308°C |
| Sn95Ag4Zn1 | -------- | 217°C | **Au80Sn20** | **280°C** | **280°C** |
| Sn93Ag5Cu2 | 216°C | 216°C | Pb90In10 | 290°C | 300°C |
| **Sn96Ag4** | **221°C** | 221°C | **Pb92Sn5Ag2.5** | **300°C** | **310°C** |
| Sn95Cu4Ag1 | 225°C | 260°C | **Pb98Sn2Ag2.5** | **304°C** | **--------** |
| **Sn99Cu1** | **227°C** | **227°C** | Pb97Ag3 | 304°C | 304°C |
| Sn97Cu3 | 227°C | 330°C | **Pb95Sn5** | **308°C** | **312°C** |
| **Sn65Ag25Sb10** | **-------** | **233°C** | **Au88Ge12** | **356°C** | **356°C** |
| Sn95Pb5 | 233°C | -------- | **Au97Si3** | **363°C** | **363°C** |

[H. Manko, *Solders and Soldering*, Third Edition, McGraw-Hill, New York, 1992.]
[N.C. Lee, *Getting ready for lead-free solders*, Proc. SMTA Learning Institute, Ellicott City, MD, April 1997.]
[M. Pecht, *IC, Hybrid, and Multichip Module Package Design Guidelines*, John Wiley and Sons, New York, 1994.]
[D. Frear, "High Temperature Solder Materials and Conductive Adhesives," in *High Temperature Electronics*, P. McCluskey, R. Grzybowski, and T. Podlesak, eds., CRC Press, Boca Raton, FL, 1996 (in press).]

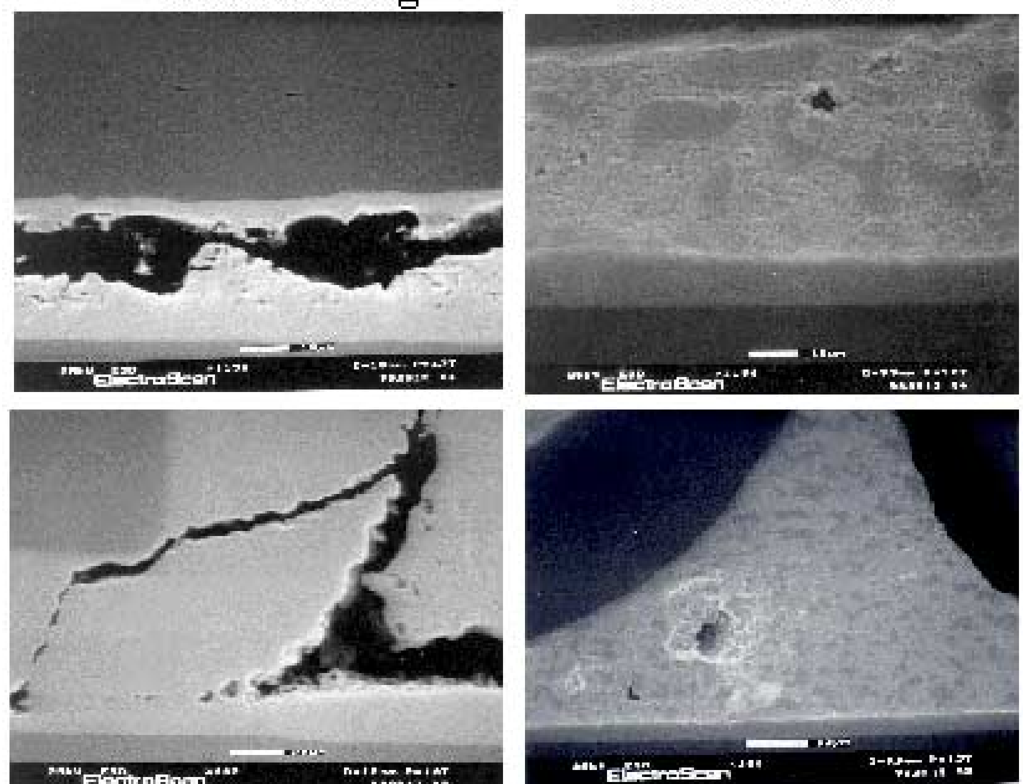
# High –Temp Solders for Interconnects

- Assemblies with two types of solders (high-tin and high-lead) were aged for 500 hrs at 185 deg C and temperature cycled between $-25^0$ to $175^0$ C.
- Results below show intermetallic growth and associated weakening in the the high-tin solder (Ni/Pd/Au plating for for high-tin solder and Sn/Pb plating for high Pb solder).

interconnect formation/reliability



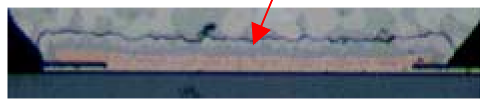

96.5Sn-3.5Ag 85Pb-10Sb-5Sn

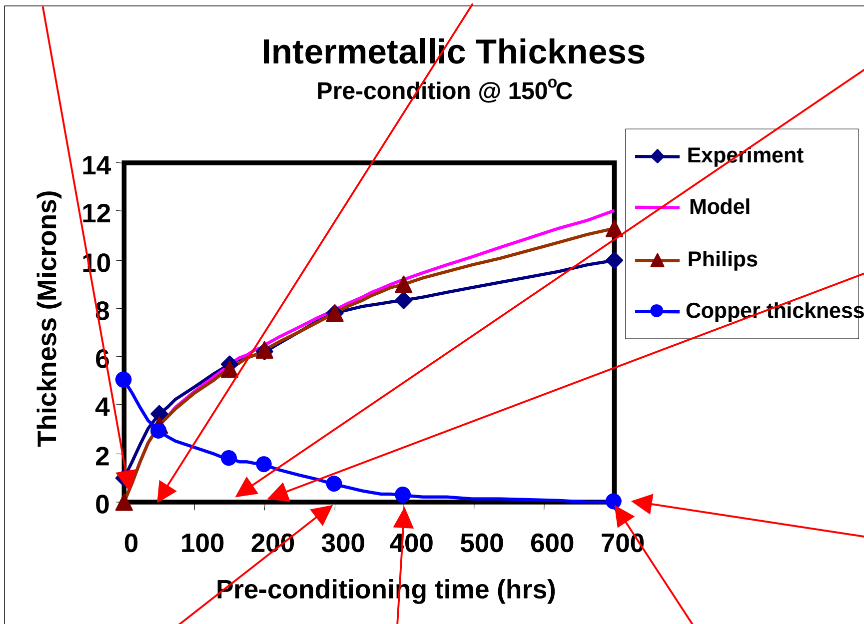


63Sn37Pb solder
Intermetallic

Cu pad
5 microns
Si die

Intermetallic
compound



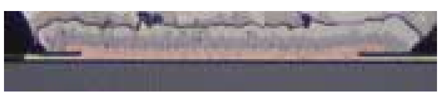


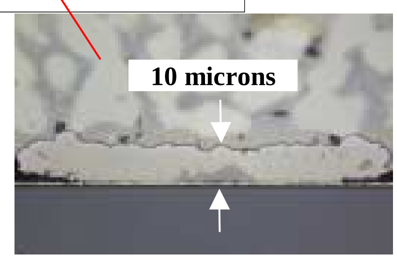

η - Phase $Cu_6Sn_5$

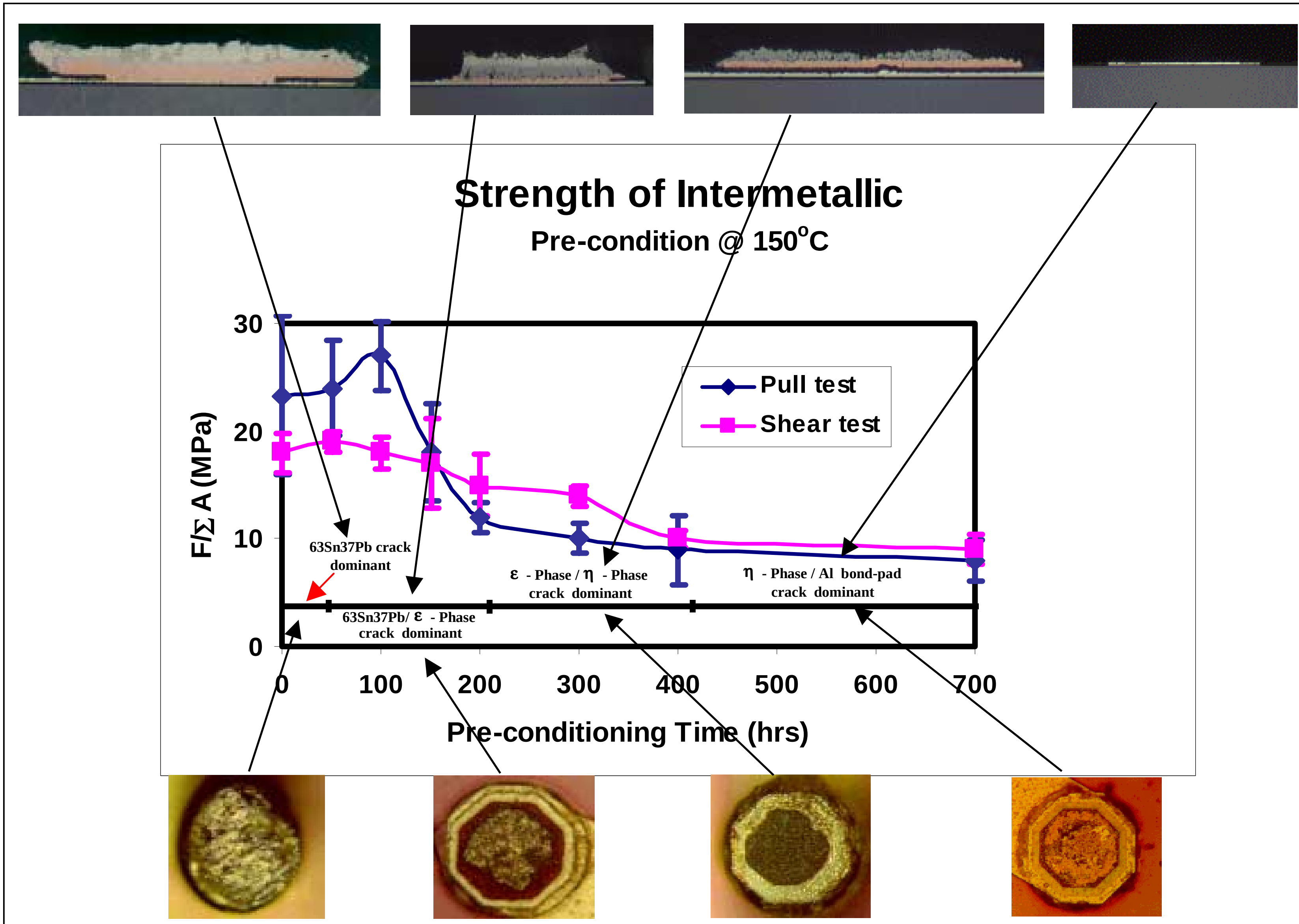
ε - Phase $Cu_3Sn$

$$z^2 = D_0 t \exp\left(-\frac{Q}{RT}\right)$$

Z= intermetallic thickness
t= aging time
Do= diffusion coefficient
T= absolute temperature
Q= activation energy
R= gas constant




Strength of Intermetallic
Pre-condition @ 150°C
F/Σ A (MPa)
Pre-conditioning Time (hrs)
0
10
20
30
0
100
200
300
400
500
600
700
Pull test
Shear test
63Sn37Pb crack dominant
63Sn37Pb/ ε - Phase crack dominant
ε - Phase / η - Phase crack dominant
η - Phase / Al bond-pad crack dominant

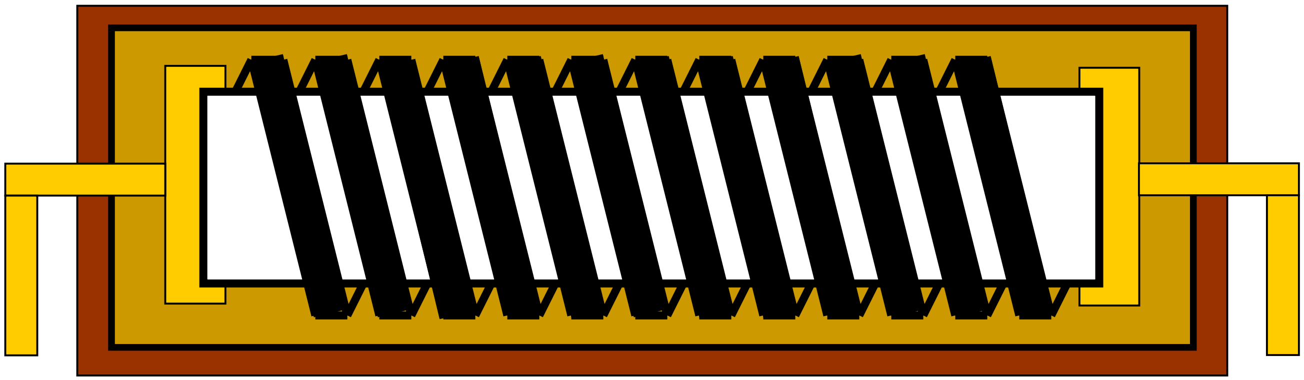
# Electrically conductive adhesives

- Some silver filled polyimide and epoxy conductive adhesives can be used to temperatures of 200C to 250C
- Fewer processing steps, but rework is difficult for thermosetting adhesives, and the cost is higher
- Thermal aging can strengthen adhesives by additional curing
- Aging in presence of moisture can oxidize the metal decreasing joint strength, adhesion, and electrical conductivity
- Moisture in the presence of ions can lead to silver migration
- High susceptibility to thermomechanical fatigue with even small CTE differences. Higher temperature adhesives are less compliant and more brittle with lower fatigue resistance.

# Separable Connectors

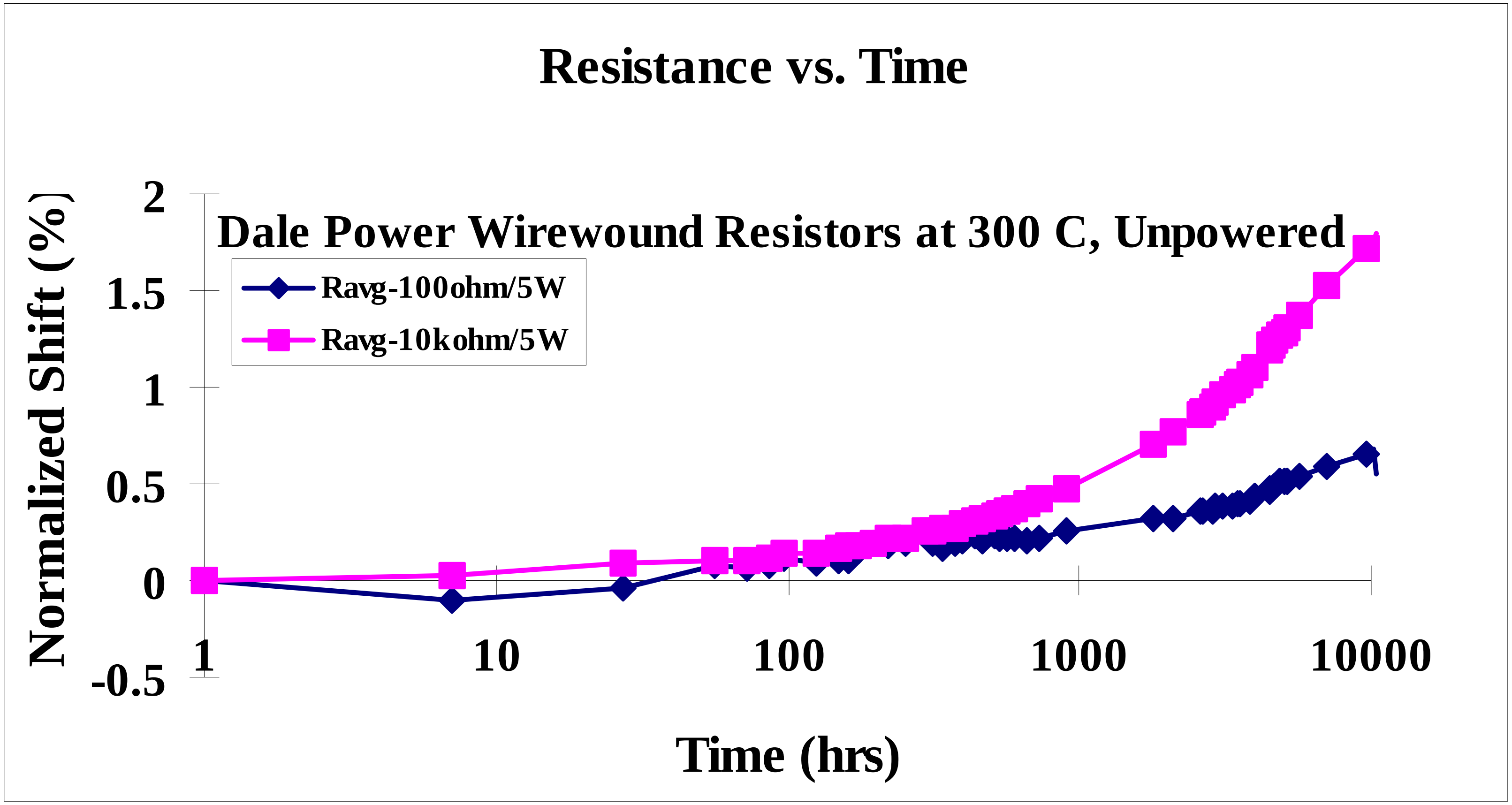
- Spring Materials
  - Main failure mechanism is by stress relaxation
  - Beryllium copper is good to 175°C - 200°C
  - Beryllium nickel is good to 300°C
- Platings
  - Soft gold will work to 200°C
  - Migration of impurities in hard gold cause failure at temperatures below 200°C
  - Tin lead is not useful above 125°C

# Wire wound resistor



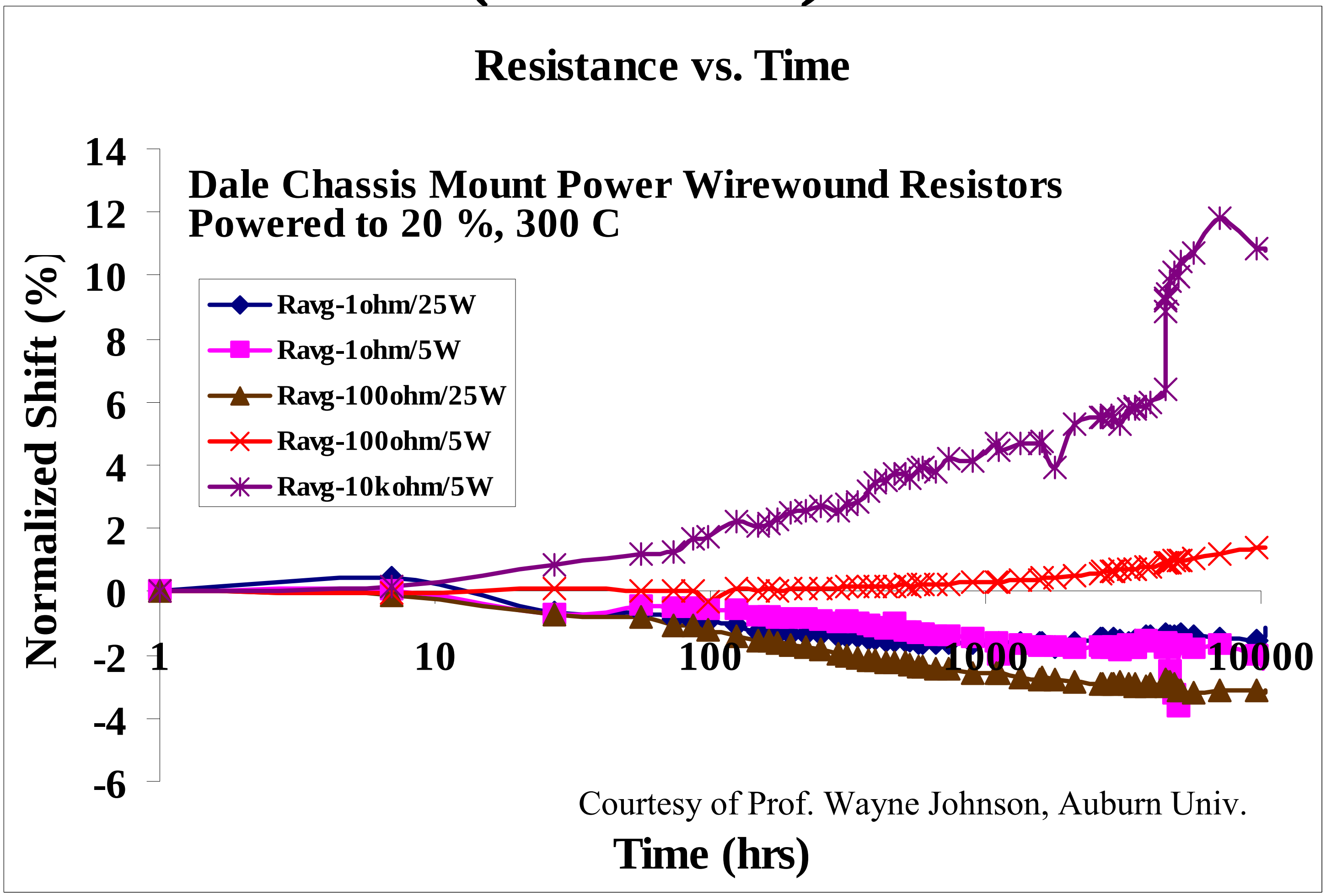
- **Resistive wire: Ni-Cr, Cu-Ni, Cu-Mn, Fe-Cr with a Teflon™ PTFE insulation**
- **Diallyl phthalate (DAP) or alumina bobbin**
- **Au plated nickel axial leads and end caps**
- **Moldable plastic encapsulant inside shell**
- **High precision, high cost**
- **High power (> 1 watt dissipation)**
- **Good temperature stability**

# *300°C Power Wirewound Storage Plots (Unpowered)*

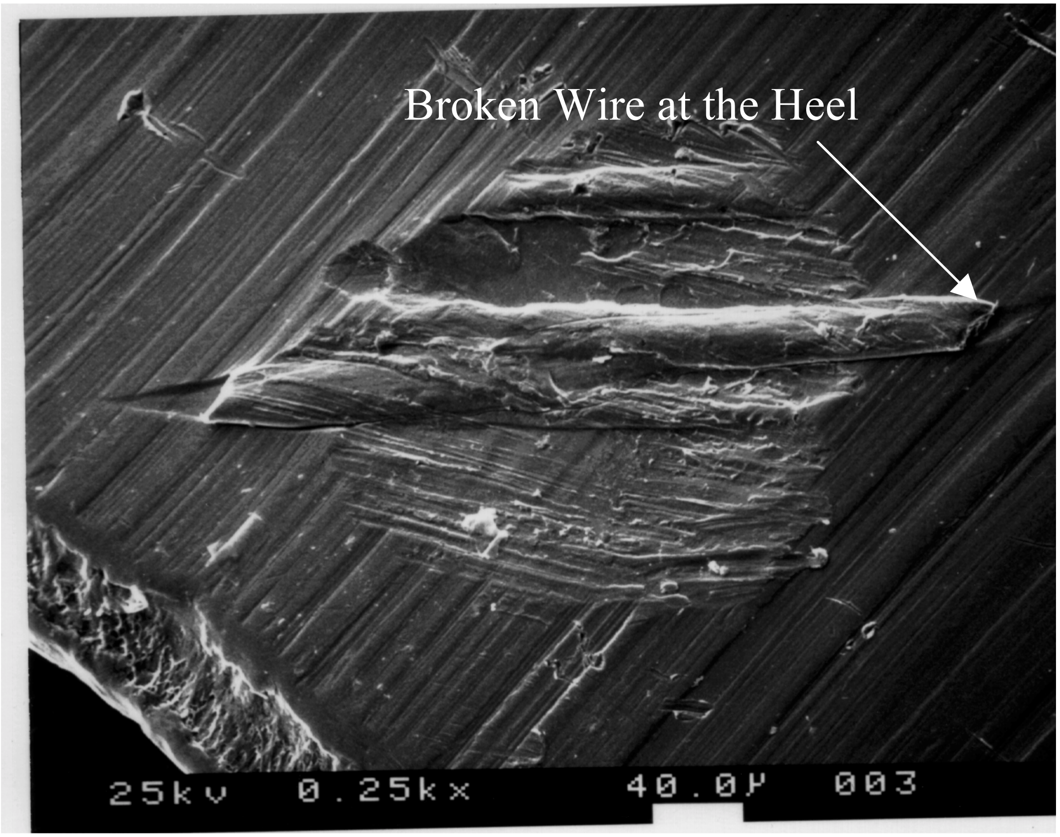



Courtesy of Prof. Wayne Johnson, Auburn Univ.

# 300°C Power Wirewound Storage Plots (Powered)



# *Failed Wire: Aged 10KΩ/5W Dale Resistor after 100 Thermal Cycles (-55 ℃ to 225 ℃)*

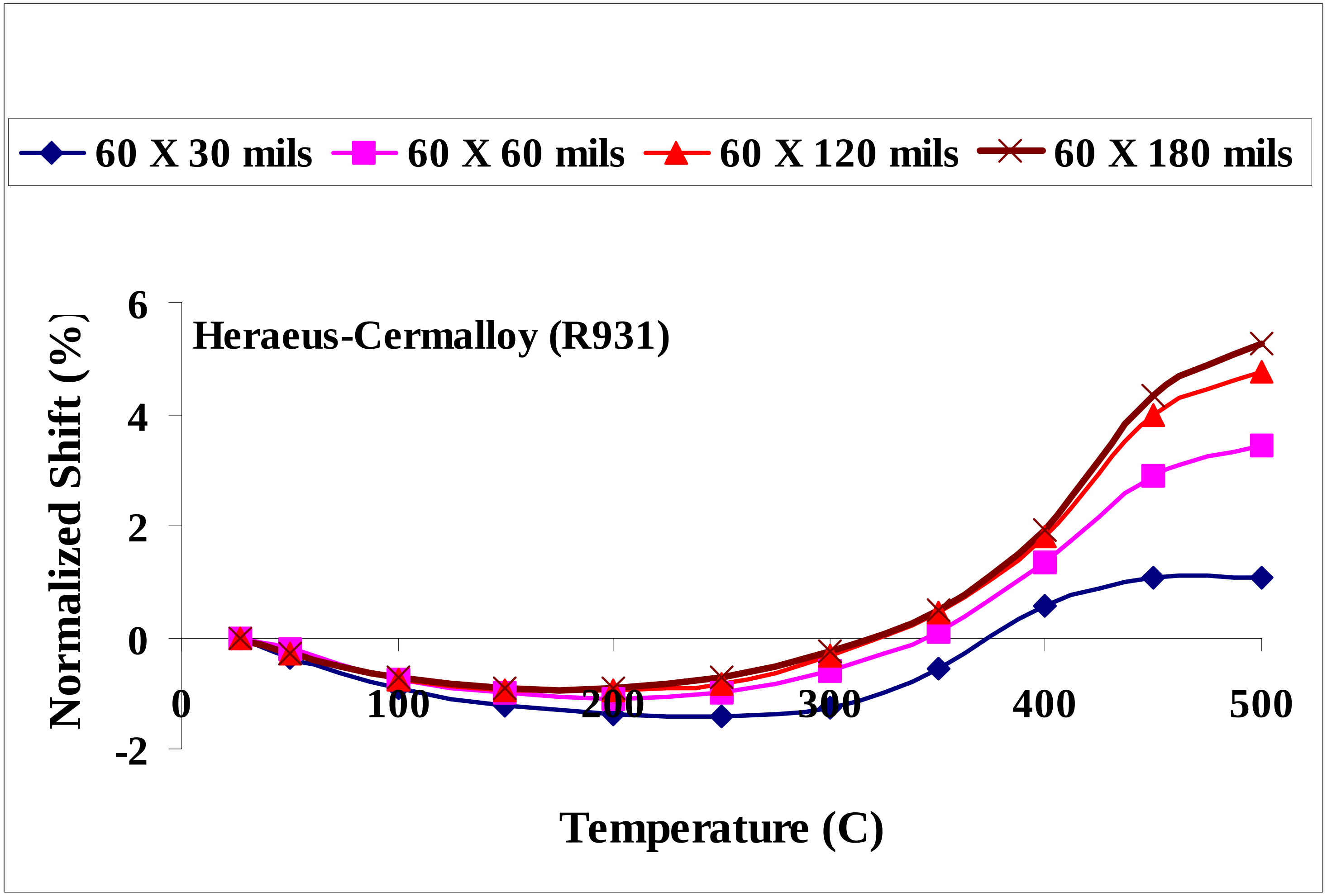



Courtesy of Prof. Wayne Johnson, Auburn Univ.

# Rectangular chip resistor (SMT)

- **Alumina ($Al_2O_3$) insulating ceramic base**
- **Thin film: Vacuum deposited film of Ni-Cr, TaN**
- **Thick film: Fired paste of $RuO_2$**
- **Silver inner electrode/Nickel outer electrode**
- **Overplate with Sn37Pb solder leadless contact pads**
- **Small size**
- **Small power, good temperature stability**

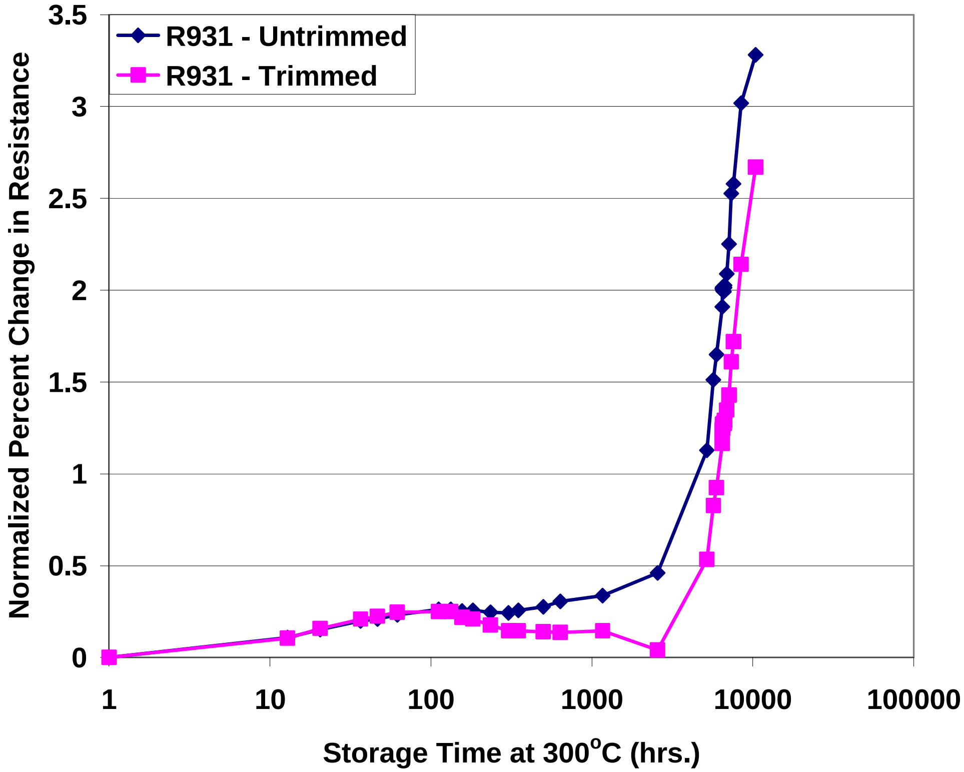
# *TCR- Thick Film - 1 kΩ/□*

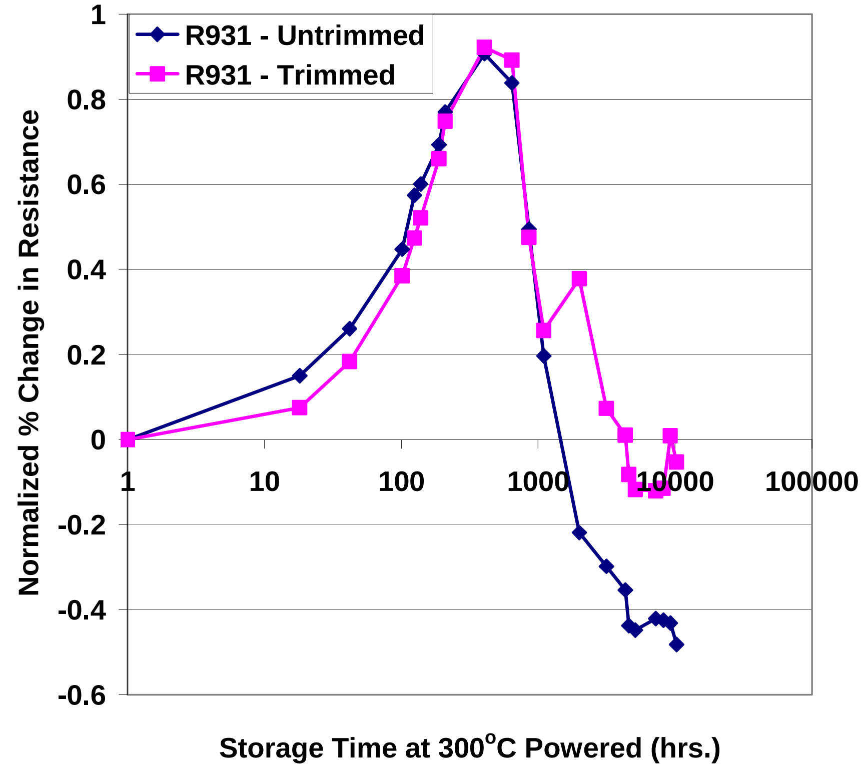



Courtesy of Prof. Wayne Johnson, Auburn Univ.

# *300°C Thick Film R931-1 kΩ/□*

- **Unpowered - PdAg Terminations**
- **Powered 1/8W - Au Terminations**



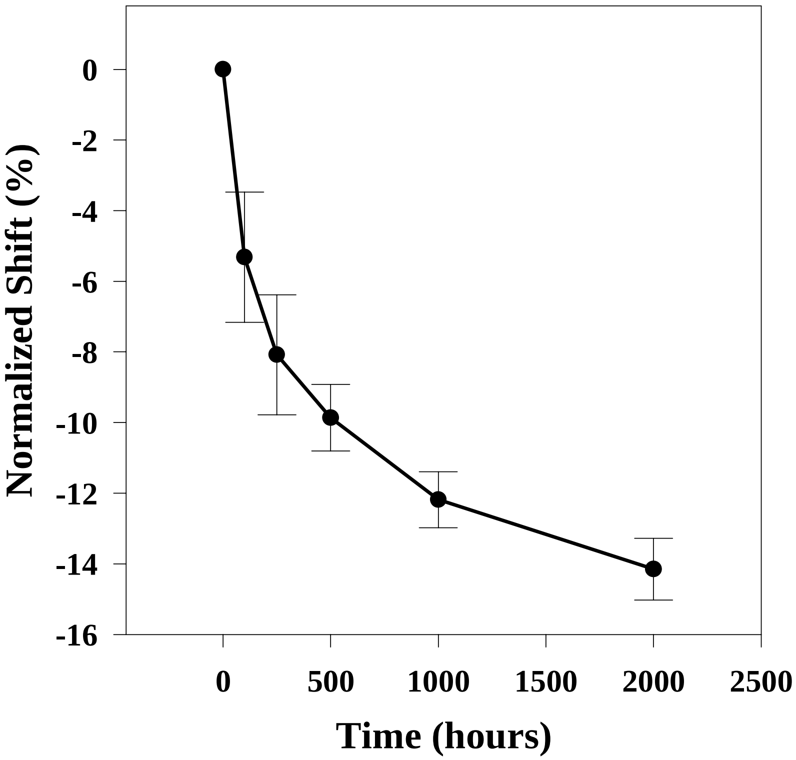



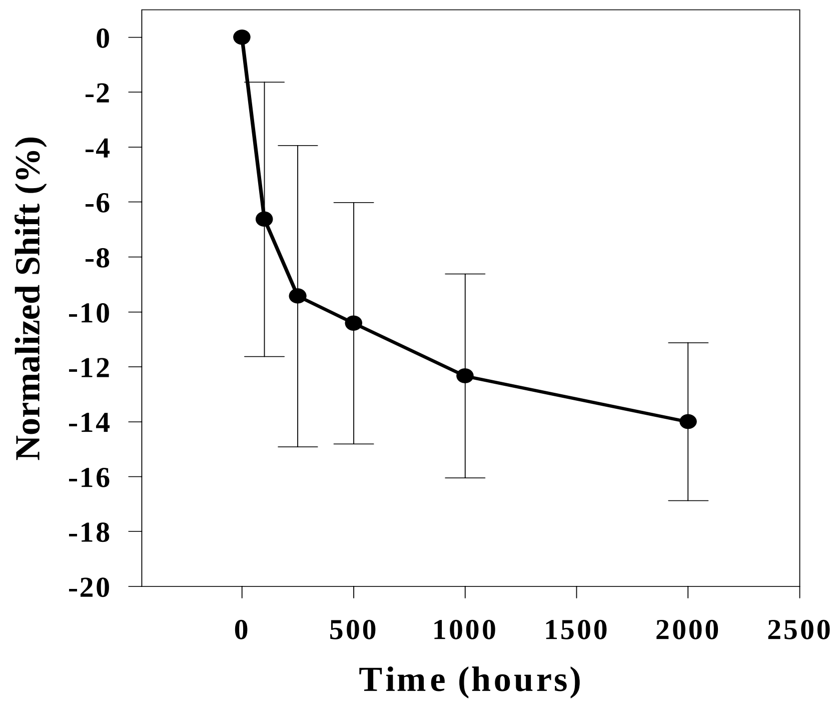

Courtesy of Prof. Wayne Johnson, Auburn Univ.

# 500°C Thick Film

## (Powered - Au) R941-100 Ω/☐

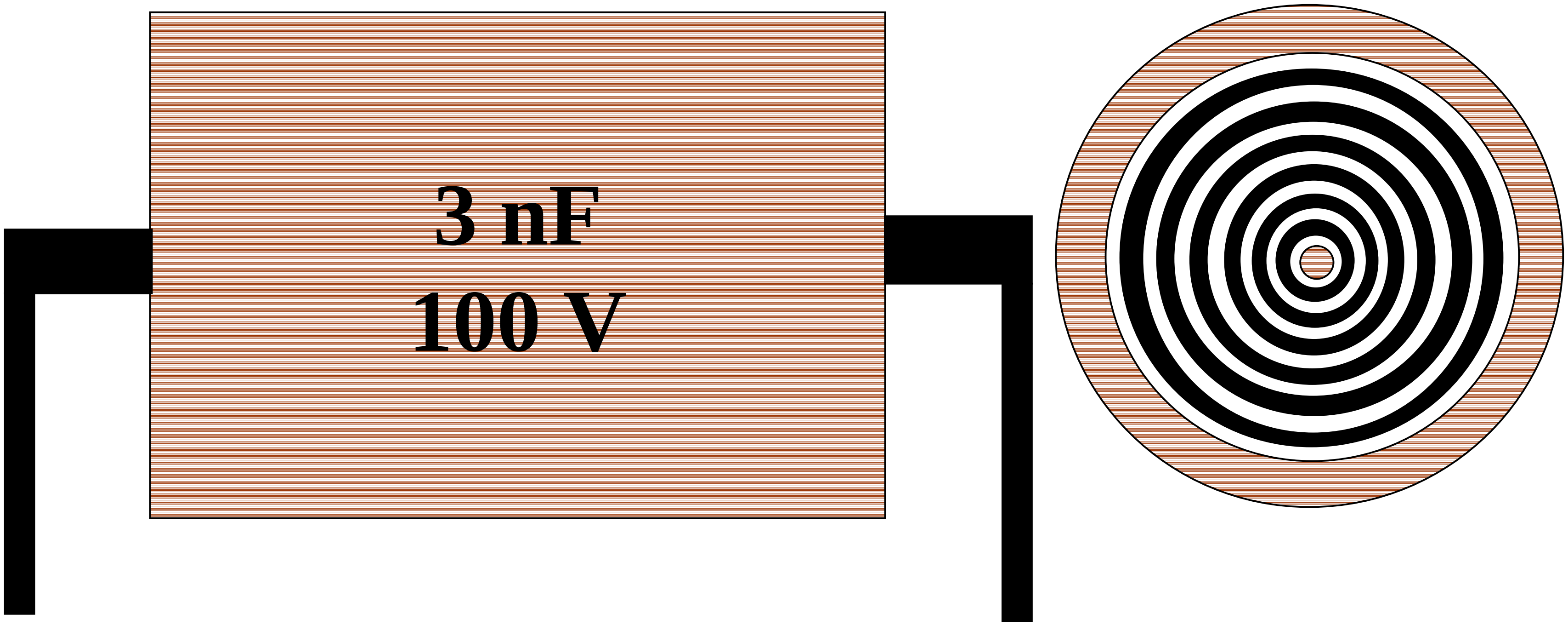
- **Untrimmed**
- **Trimmed**



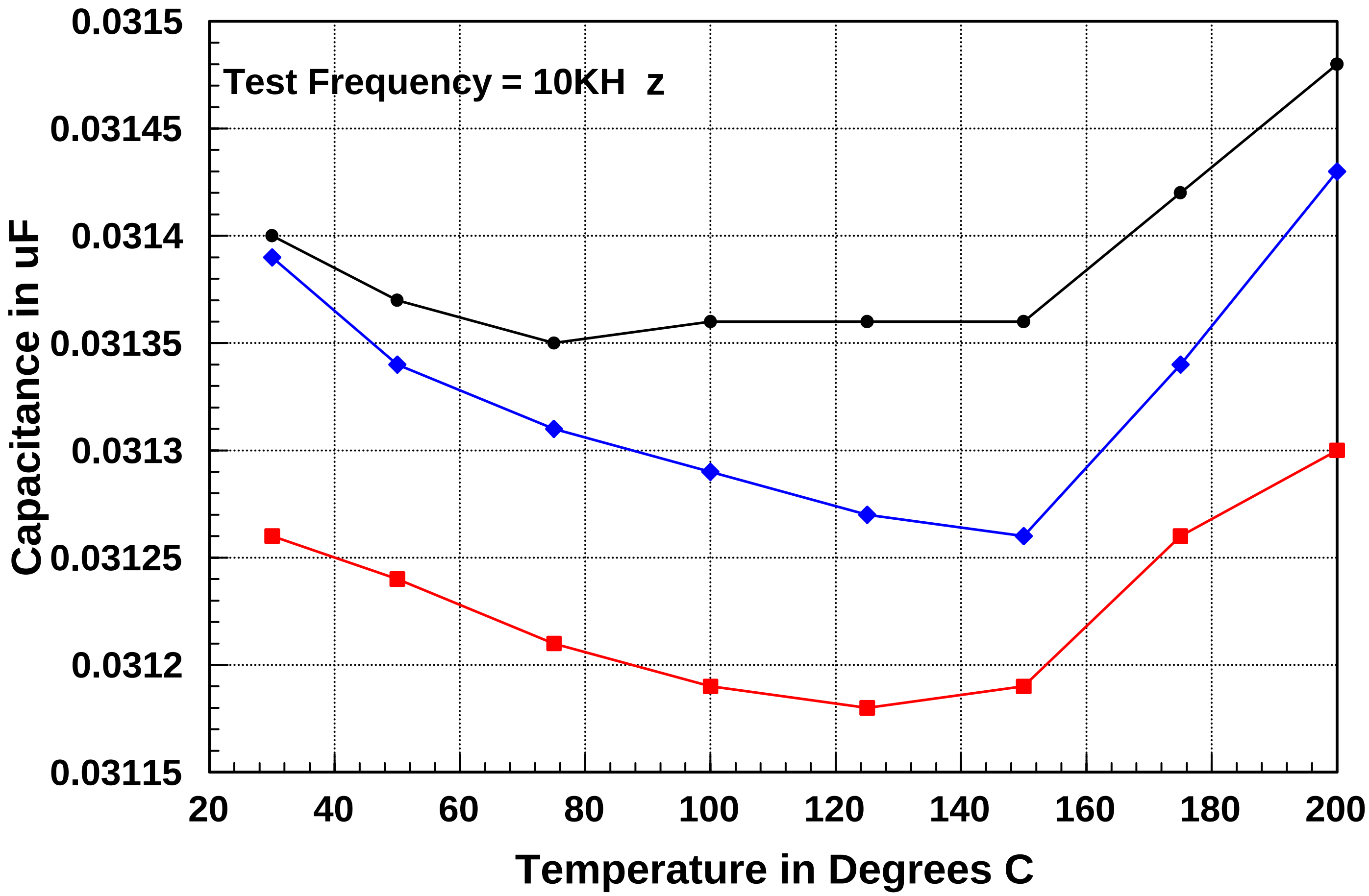

Courtesy of Prof. Wayne Johnson, Auburn Univ.

# Axial Polymer Capacitor



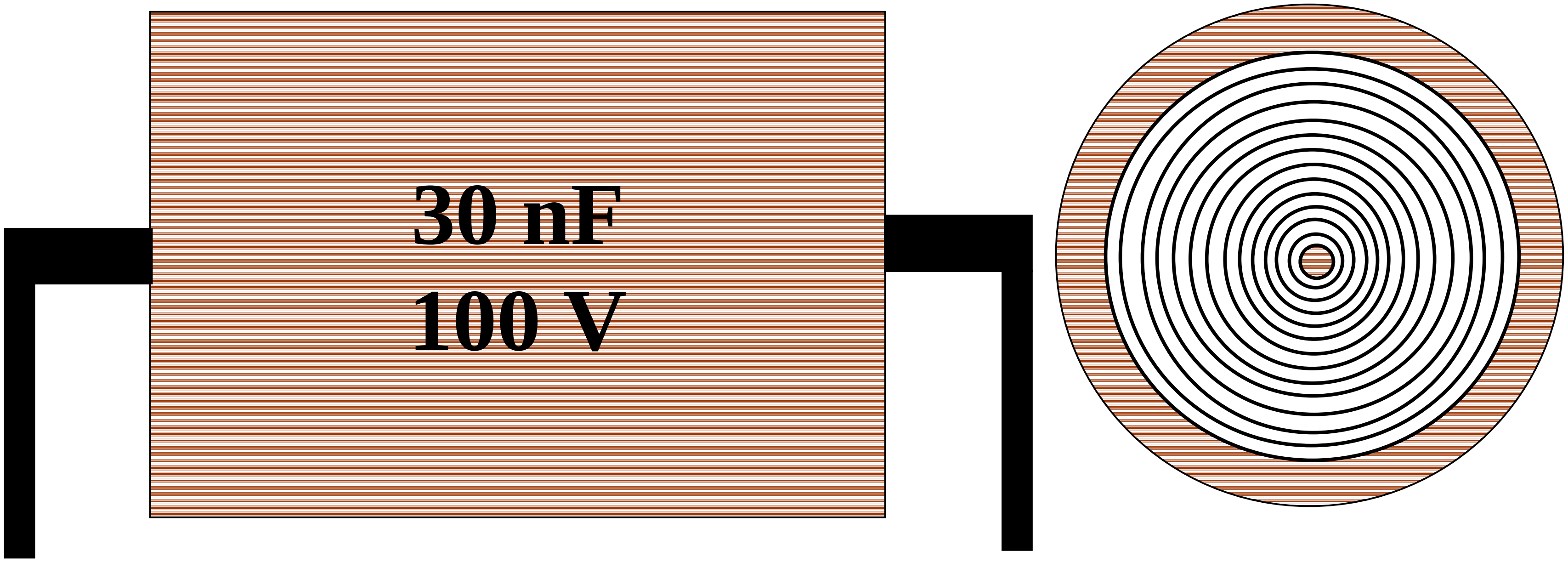

- Alternating layers of metal foil and polymer foil are rolled into a cylinder and connected to leads.
- Epoxy encapsulant
- Poor temperature stability except for teflon

# Custom Electronics Teflon Capacitor (TFHT0137) .033uF +/- 10%, 600 WVDC Capacitance vs. Temperature



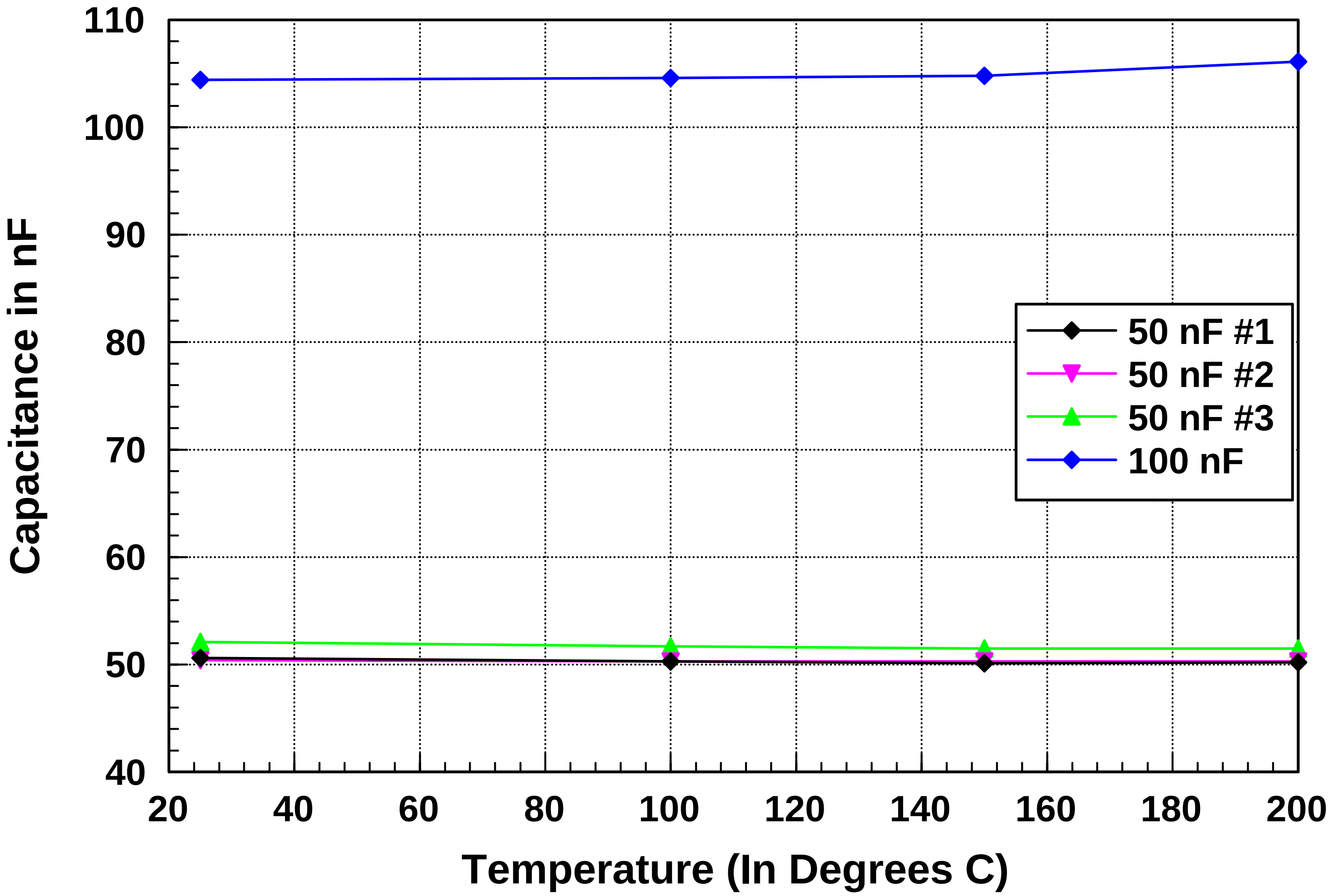

Courtesy of Dr. Richard Grzybowski and United Technologies

# Metallized Film Capacitor



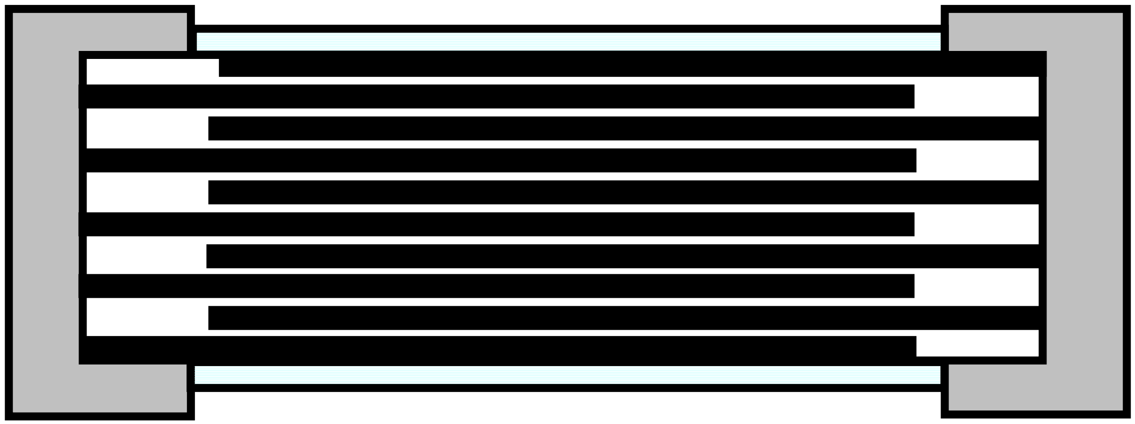

- **Polymer film is coated with a resistive metal coating, rolled into a cylinder and connected to leads.**
- **The thin resistive metal coating permits more layers and therefore more capacitance.**
- **The thin resistive metal coating permits self-healing.**
- **Epoxy encapsulant**
- **Poor temperature stability except for teflon**

# Custom Electronics Metallized Teflon Capacitors 200 WVDC TMHT201503J = 0.05 uF, TMHT201104J = 0.1 uF




Courtesy of Dr. Richard Grzybowski and United Technologies

# Multilayer ceramic chip capacitor

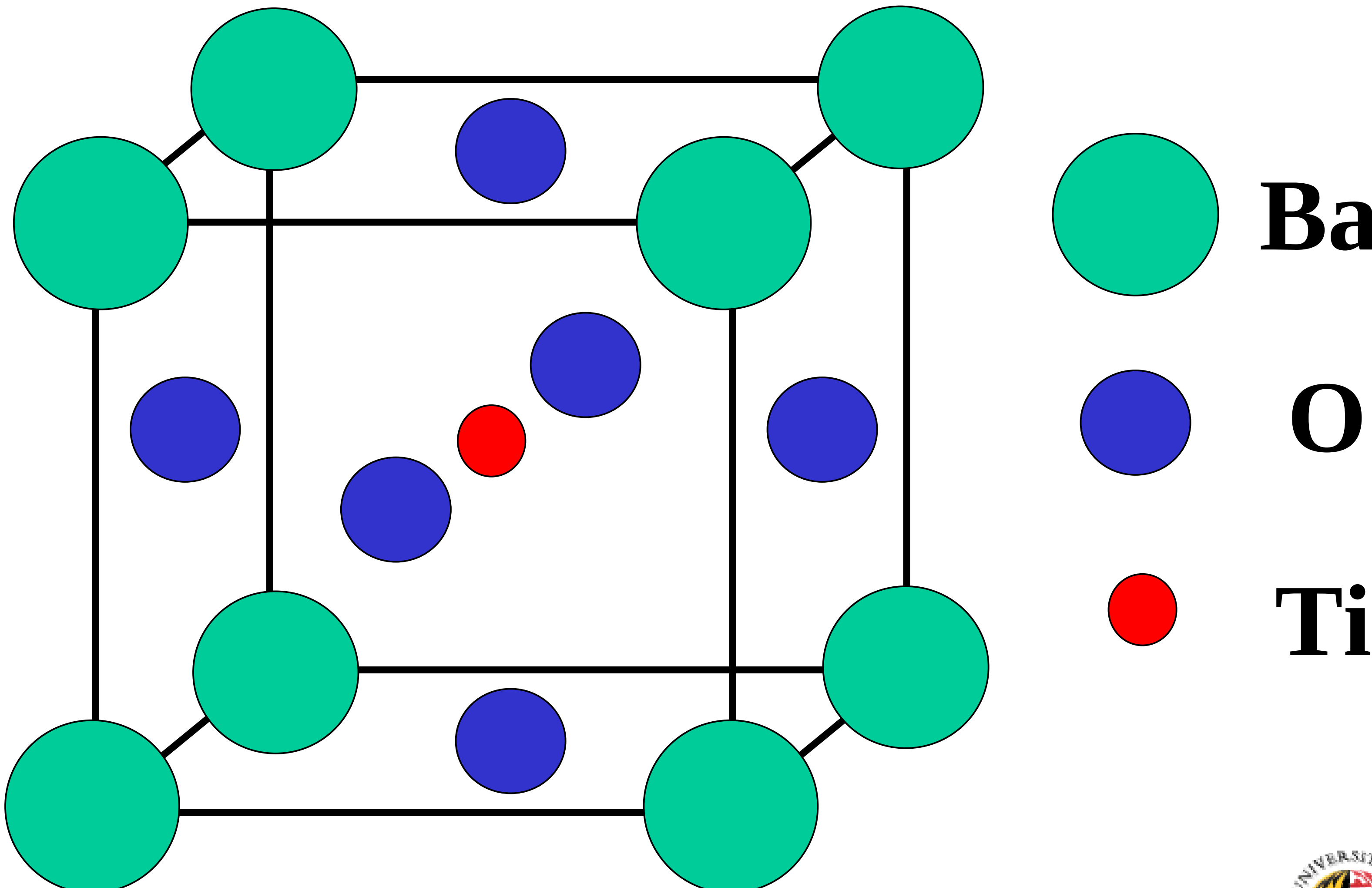


- **Insulating and capacitive base.**
- **Multiple layers of conductive material increase the area of the electrodes while minimizing the thickness of the ceramic, thereby increasing the capacitance.**
- **Nickel over silver leadless contact pads.**
- **Small size.**
- **Higher capacitance/good temperature stability**

# Capacitor Materials

- **Insulating materials are used between the capacitor plates to increase the charge that can be held on the plates, thus providing a dielectric constant greater than that for vacuum, $\varepsilon_r = 1$**
- **Alumina ($Al_2O_3$) or silica ($SiO_2$) ceramics have the smallest dielectric constants ($\varepsilon_r$ = 4 to 10) but the highest temperature stability.**
- **Barium titanate ($BaTiO_3$) and other perovskites (PZT – $Pb(ZrO_3/TiO_3)$) have the highest dielectric constants ($\varepsilon_r$ = 1000+) but the lowest temperature stability.**

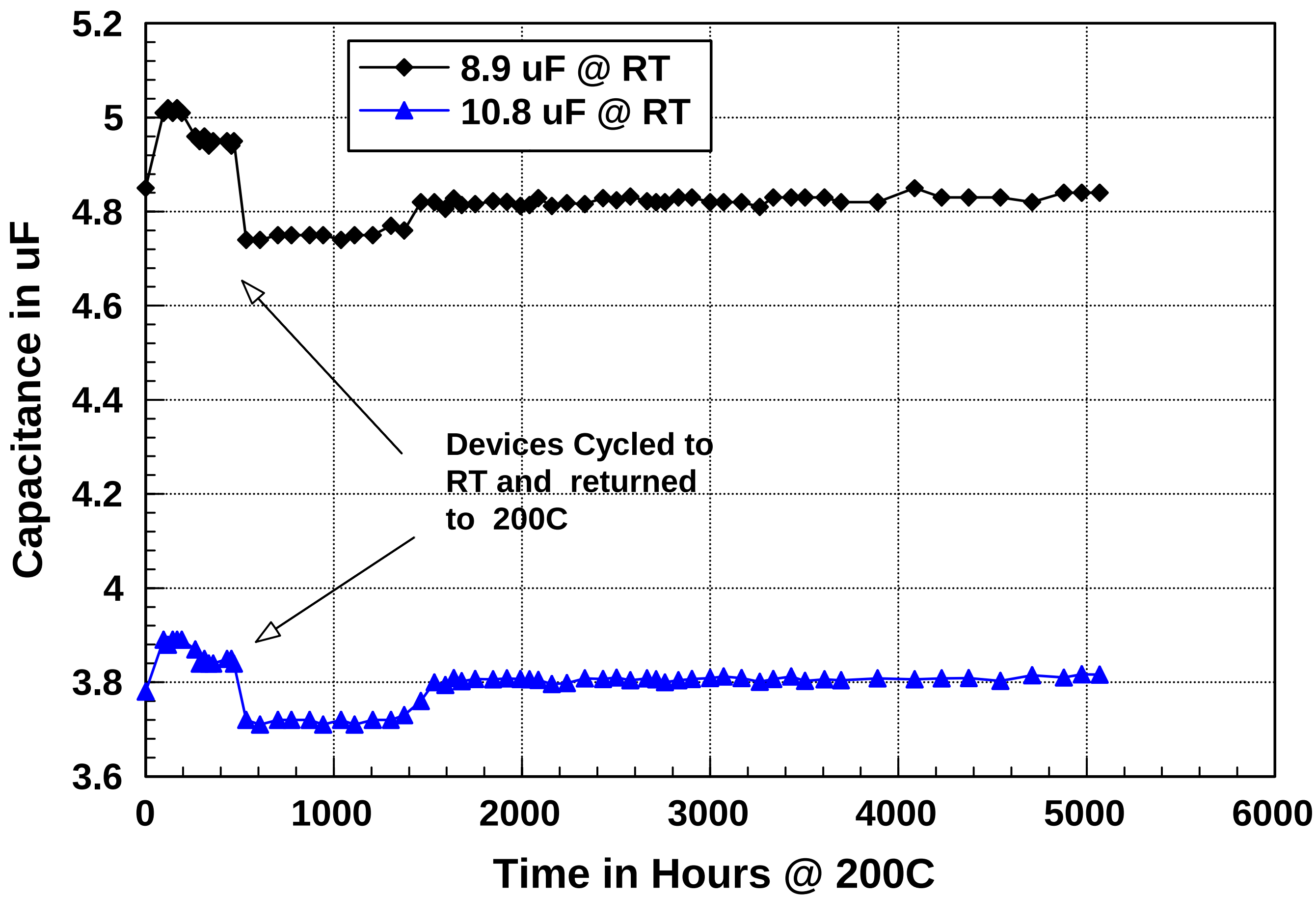
# Perovskite Structure ($BaTiO_3$)



# Common $BaTiO_3$ Formulations

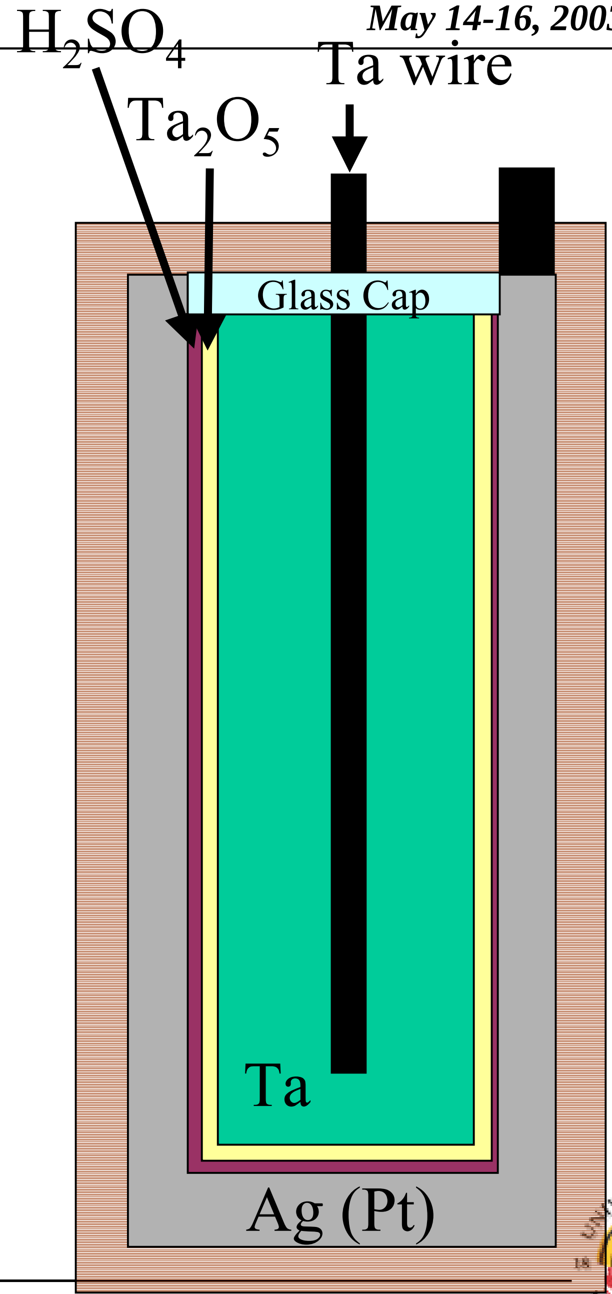
- **NP0 – a $Ba(TiO_3)_4$ formulation that has a zero temperature coefficient of capacitance for a wide range of temperatures above and below room temperature and is stable up to T=500°C.**
- **X7R – The most common $BaTiO_3/SiO_2$ based formulation. Capacitance is fairly stable (slightly increasing) with temperature to T = 150°C.**
- **Z5U – A less common $BaTiO_3/SiO_2$ formulation that has high capacitance with wide fluctuations above and below room temperature.**

# NOVA X7R Capacitors Aged At 200C

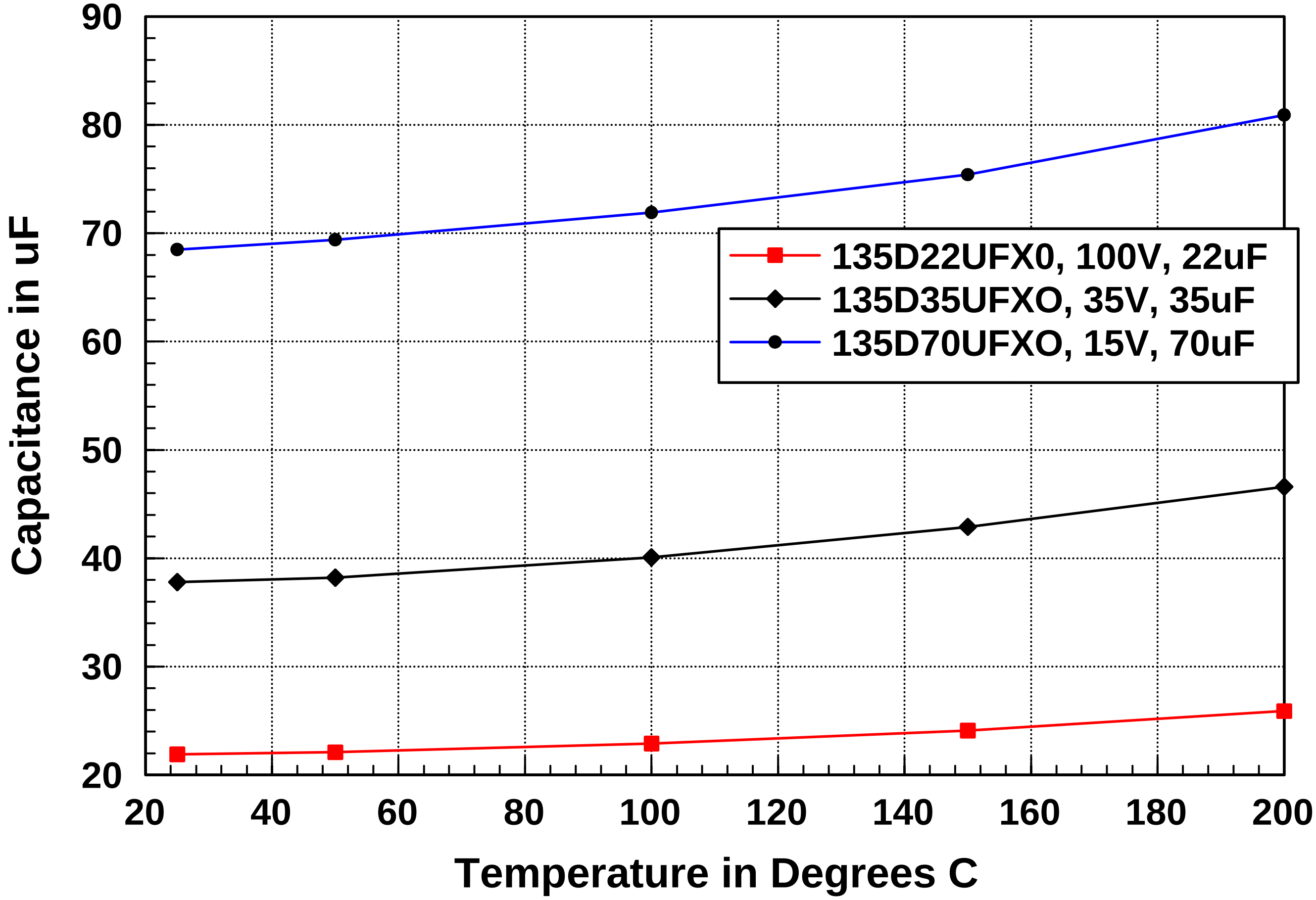


# Wet electrolytic capacitor

- A thin capacitive film is created by an oxidation reaction between a metal and a liquid electrolyte.
- The film has a large area due to the rough surface of the metal and a small thickness leading to high capacitance.
- Capacitors can fail by dryout.
- High power
- Poor temperature stability



# Sprague Wet Tantalum Capacitors With 6V DC Bias, F=1KHz @ 1Vrms




Courtesy of Dr. Richard Grzybowski and United Technologies

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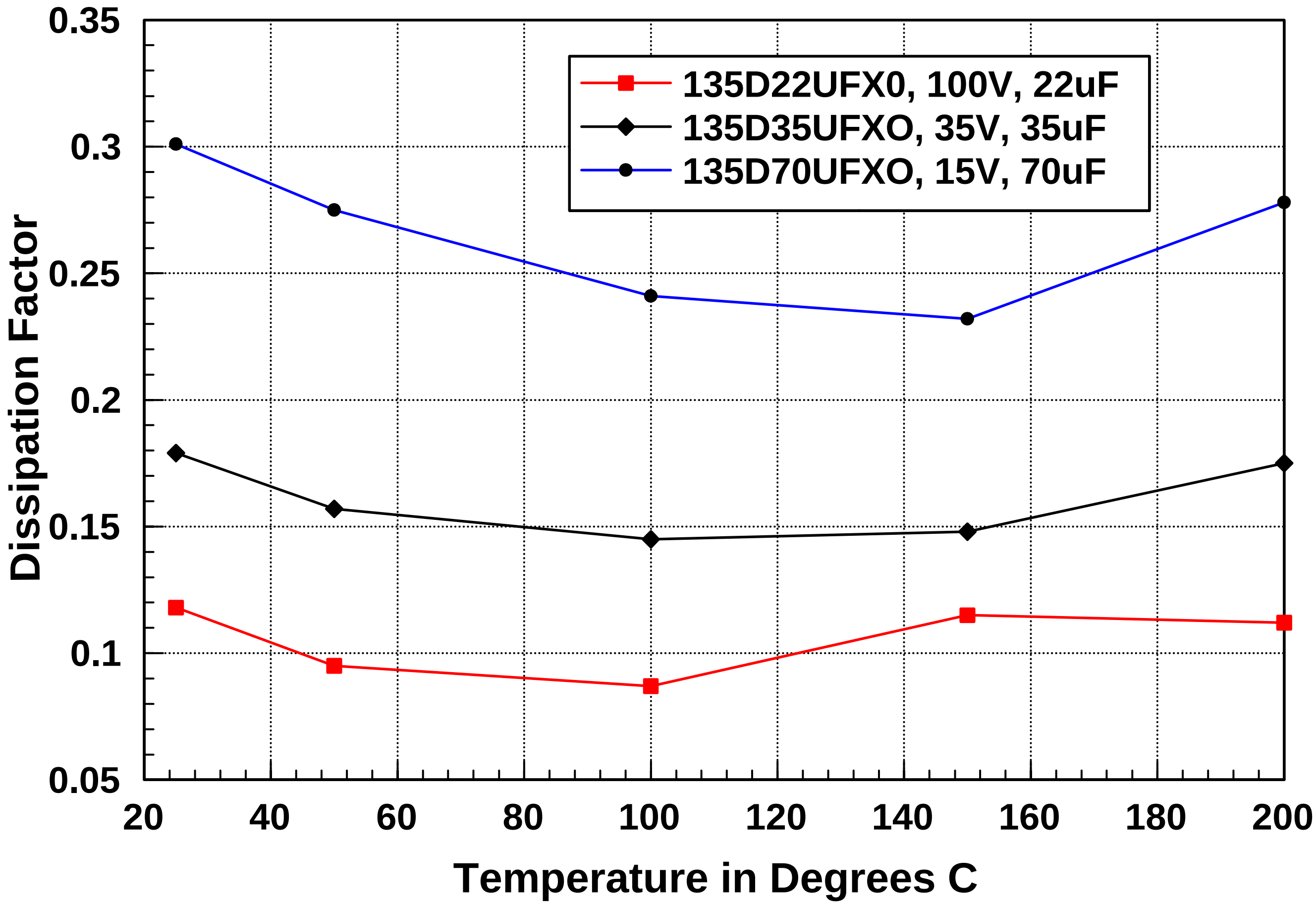


Courtesy of Dr. Richard Grzybowski and United Technologies

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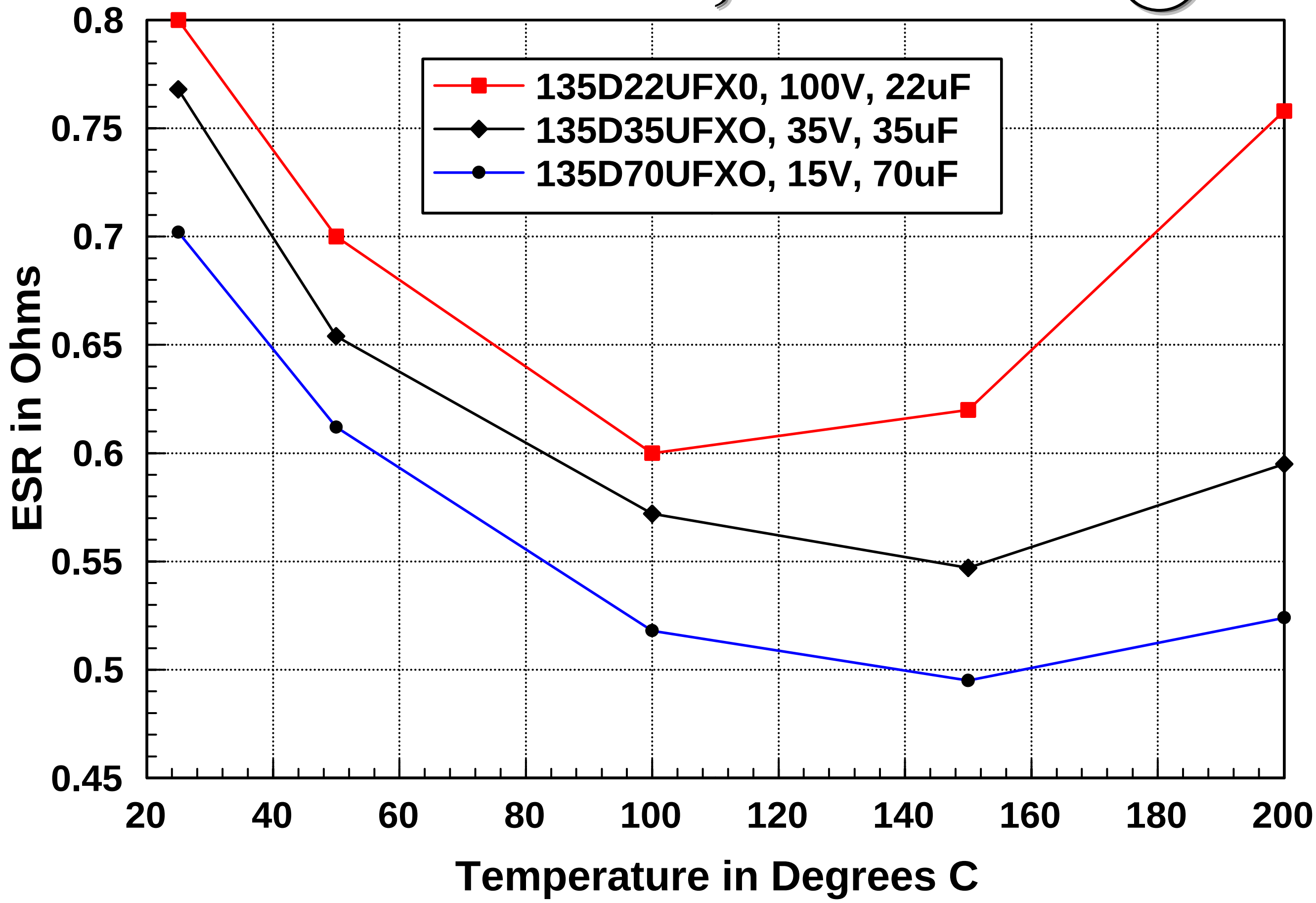
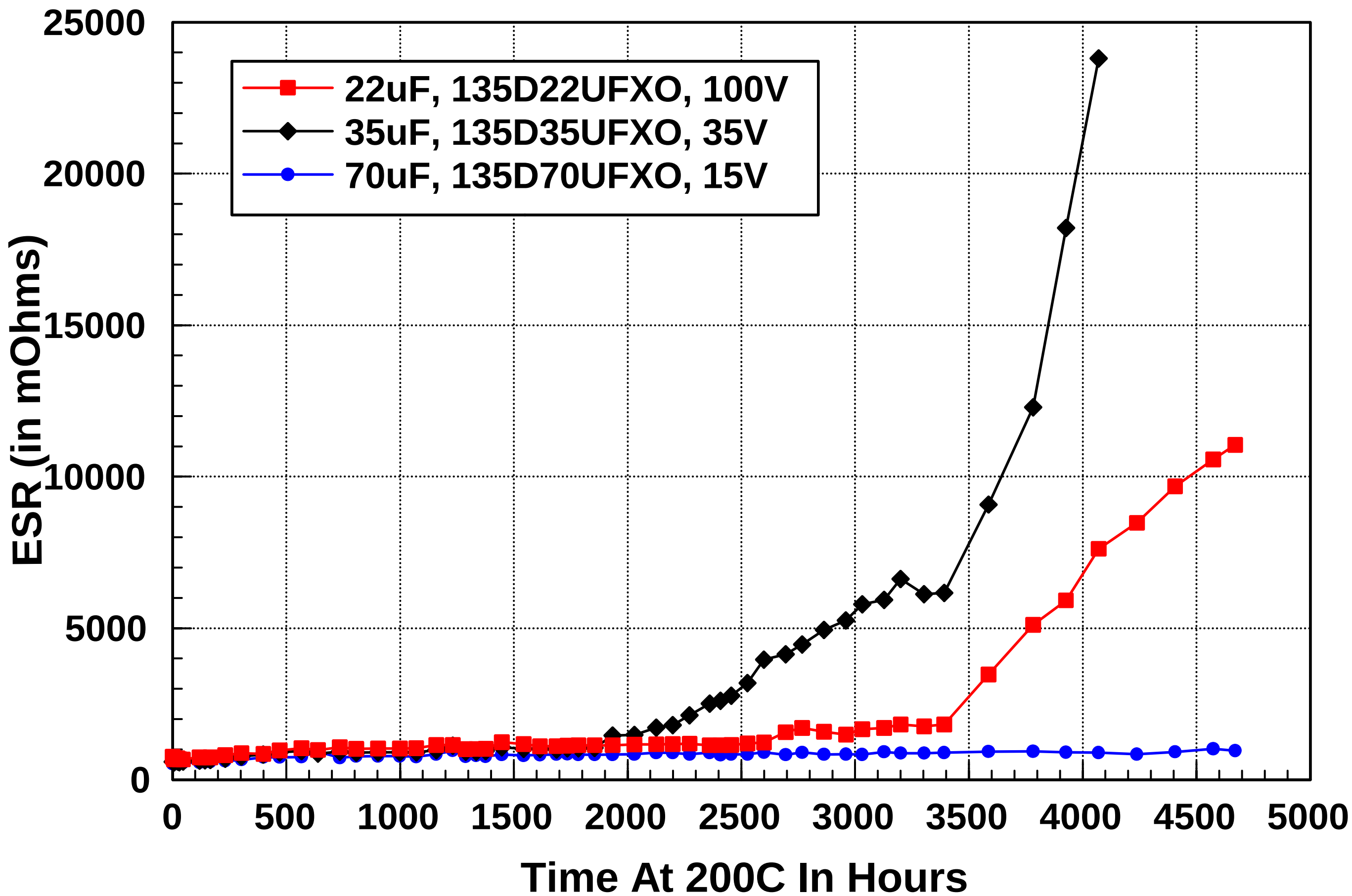



Courtesy of Dr. Richard Grzybowski and United Technologies

# Sprague Wet Tantalum Capacitors

# 6V DC Bias at 1KHz / 1Vrms




Courtesy of Dr. Richard Grzybowski and United Technologies

# Passives – Vendor Issues

- Most systems integrators are NOT in the passive components manufacturing business.
- If a component manufacturer wants to make harsh environment components one of their niches - a symbiotic relationship may exist:
  - If the represented market is large enough (military, commercial/industrial, automotive, commodity?)
  - May depend on how substantial the required process changes are from manufacturers current practice (modification or new product)
  - May depend on how much of the required expertise the system integrator brings to the partnership (can you get them started?)

# Summary of high temperature effects

- No plastic encapsulated microcircuits can be used above 180°C.
- No gold-aluminum wirebonds can be used above 180°C
- Al-Al and Al-Ni systems can be used to 300°C, but beware of fatigue in wires less than 125 μm in diameter.
- Au-Au and Au-Pt systems can be used above 300°C.
- Flip chip approaches cannot require underfill or low temperature solders and must be used with low current densities.
- Commercial metal alloy component attach can be used to 200°C.
- High lead die attach can be used to 250°C, but with fatigue issues.
- Gold-eutectic die attach can be used to 250°C – 300°C.
- Silver-glass die attach can be used above 250C for applications that do not require high backside electrical conductivity.
- Above 300°C requires high temperature brazes or monometallic solutions
- Transient liquid phase bonding has been investigated but processing times are much too slow.

# Summary of high temperature effects

- Ceramic substrates are fine as long as the thermal conductivity and CTE are considered in design.
- Thin film metallization on ceramic becomes a concern above 250°C
- Thick film metallization on ceramic good to 500°C
- DBC alumina is good but concerns about cracking in thermal cycling.
- Organic PWB are only good below 250-300°C.
- High temperature solder only good to 250°C.
- Conductive adhesives limited as well.
- Wirewound resistors good to 200C – 300C
- Thick film resistors good to 500C
- Low value capacitors (NP0 Ceramic) good to 500C
- High value capacitors are the problem - need good vendor relations