



Analog Circuit Design Techniques for Low-Temperature Mixed-Signal CMOS Systems

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Low Temperature Analog Overview



- Commercial, discrete electronics vs. Custom, monolithic systems
- System level design of low temperature analog filters and data converters
- CMOS modeling for low temperature
- Circuit topologies for low temperature analog





Commercial vs. Custom Electronics



- Commercial electronics generally perform well over a large temperature range
- Custom electronics allow high levels of integration, thus the number of individual chips is reduced and reliability is increased
- Might make sense to use some commercial electronics for some specialized functions (e.g. voltage reference)





System Level Design Considerations



- Data converter design for mixed-signal systems for low temperature environments is a challenge for several reasons:
 - Transistor characteristics change significantly with temperature ($V_{TO} \uparrow$, $\mu \uparrow$)
 - 1/f noise may be constant with temperature
 - Difficult to match a large number of passive devices over a wide range of temperatures
 - Standard reference circuits generally don't operate well over a large temperature range





System Level Design Considerations



- General data converter design approach – minimize the number of passive components required for matching

Comparison of Popular Data Converter Architectures	
Architecture	Number of components required to match one another
Flash	2^n resistors, $2^n - 1$ comparators
Successive Approximation	$3n + 1$ resistors (assuming R-2R DAC)
Pipeline/Recirculating	4 capacitors in DAC/Gain Block (assumes fully differential & 1.5 bit/stage)
Sigma-delta	4 capacitors in S.C. integrator (assumes fully differential)

- Key trade-off – pipeline and sigma-delta trade component matching for high performance op-amps – thus the converter design becomes an op-amp design problem

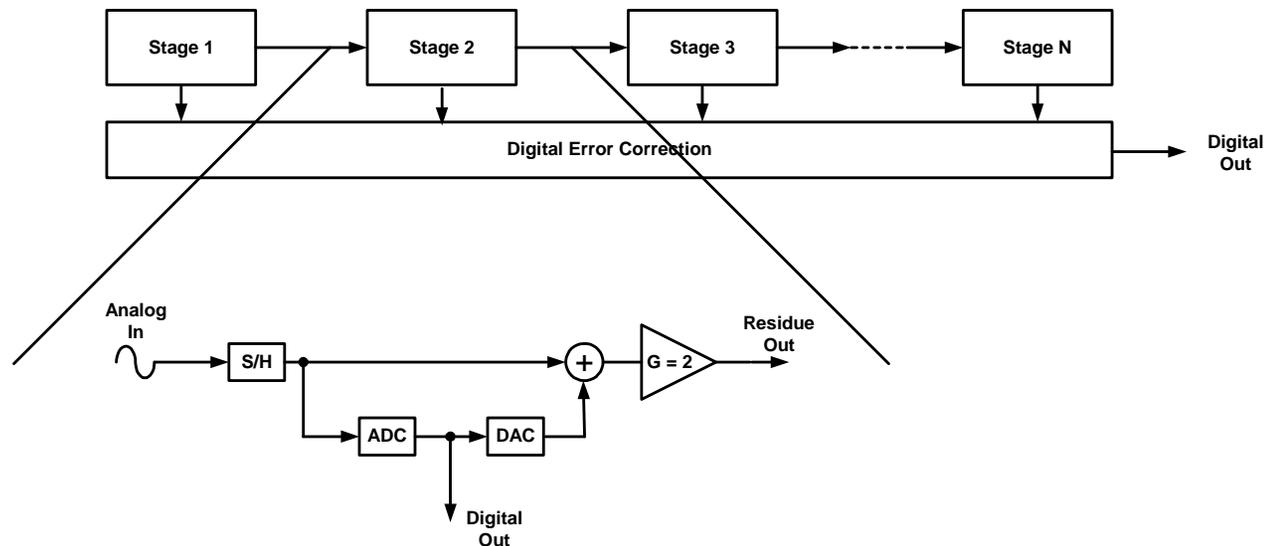




Pipeline ADC



- Pipeline ADC ideal for high-speed, moderate resolution extreme environment applications
 - Very tolerant of comparator offsets when redundancy is used
 - Matching is only required within each pipeline stage, not across the entire pipeline
 - With redundancy, resolution generally limited by noise for moderate accuracy (≤ 10 bit) applications

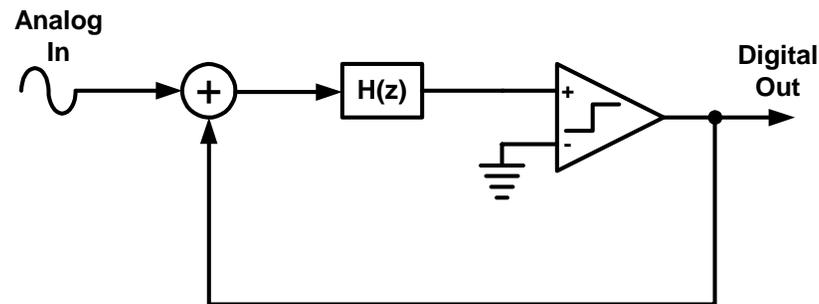




Sigma-Delta ADC



- Sigma-delta ADC is ideal for low-speed, high resolution extreme environment applications
 - $H(z)$ implemented as a switched-capacitor integrator
 - Very tolerant to comparator offset
 - Decimation filter required to convert digital output stream to digital words



- Bottom line: Sigma-Delta & Pipeline ADCs suitable for extreme environment applications require high-performance OTAs





CMOS Analog Design for Low Temp



- Important Considerations:

- Vendor models not specified at cryogenic temperatures
- Standard circuit topologies may not work over large temperature range
- Standard design equations not valid for large temperature range





Low Temperature CMOS Modeling



- Vendor supplied models generally not specified at cryogenic temperatures
- Options for low temperature modeling:
 - Extract model parameters at low temperatures (EKV might be a good option)
 - Extract critical device parameters (V_{TO} , μ) at different temperatures and create 'binned' model





CMOS Analog Design for Low Temp

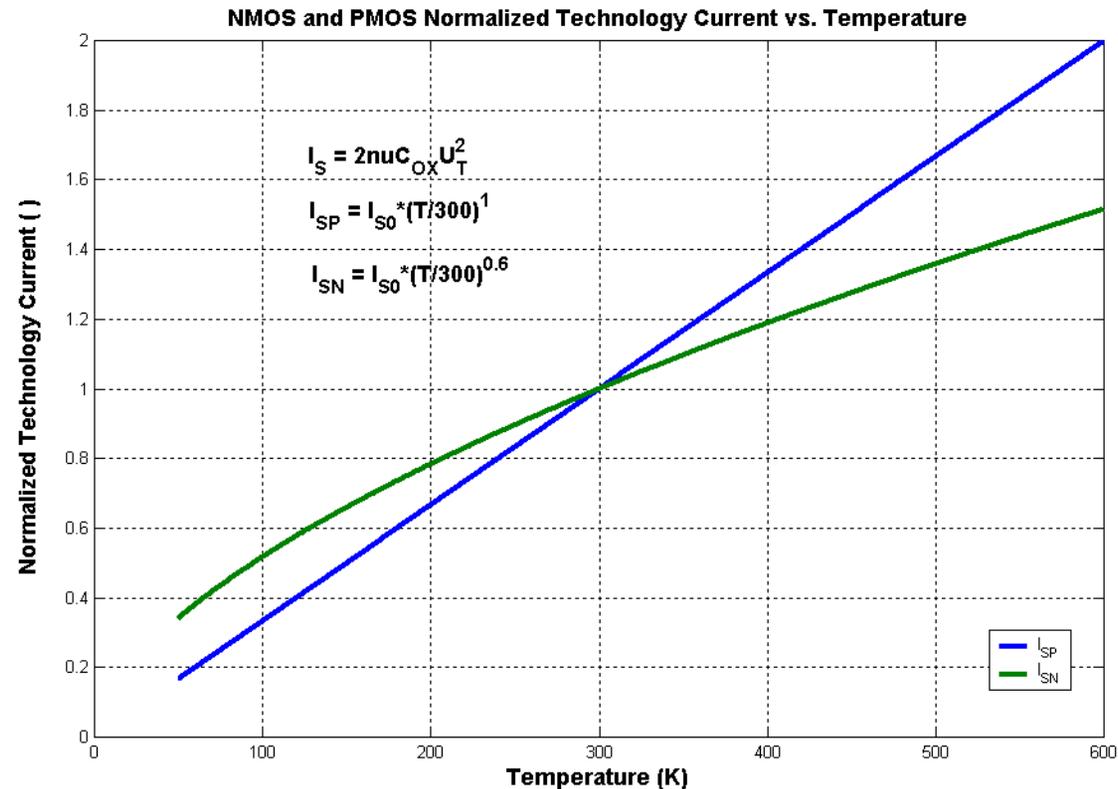


- Analog CMOS design methods normally focus on one operating region (weak, moderate, or strong inversion)
- However for a fixed bias current, operating region will change with temperature

$$U_T = \frac{kT}{q}$$

$$\mu_p = \mu_{0p} \left(\frac{T}{300} \right)^{-1}$$

$$\mu_n = \mu_{0n} \left(\frac{T}{300} \right)^{-1.4}$$

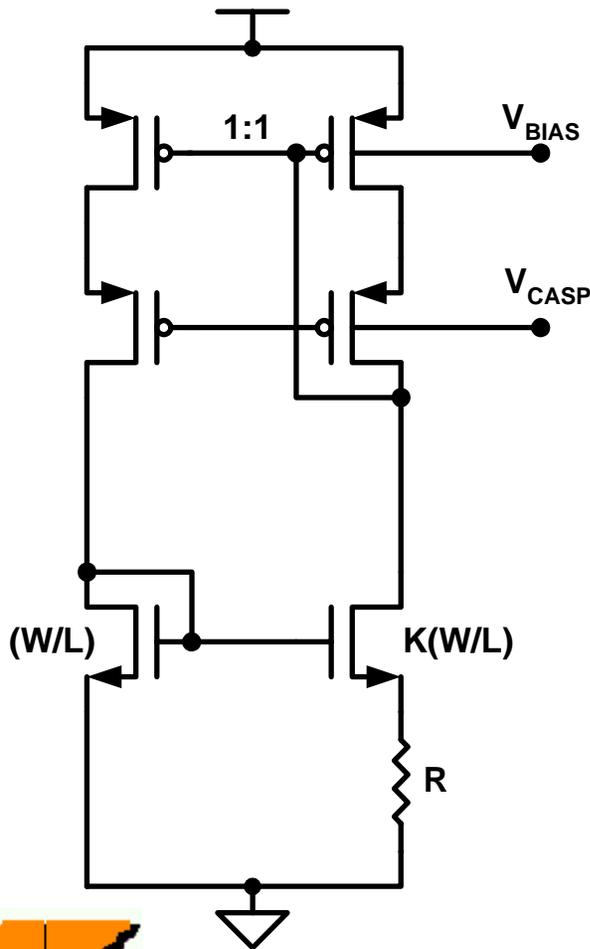




OTA Design – Constant g_m Biasing



- Constant g_m biasing is critical for regulating bandwidth and noise floor over a wide temperature range



- The Beta-multiplier is a popular constant g_m bias circuit, however the standard analysis assumes either strong or weak inversion
- Analysis of this circuit using the EKV model provides a design equation that describes operation at any inversion level (IC)

$$g_m = \left(\frac{1}{n \cdot R} \right) \left[\frac{2}{\sqrt{IC}} \cdot \ln \left(\frac{e^{\sqrt{IC}} - 1}{e^{\sqrt{IC}/K} - 1} \right) (1 - e^{-\sqrt{IC}}) \right]$$

- Choose $K \leq 2$ for low temperature sensitivity

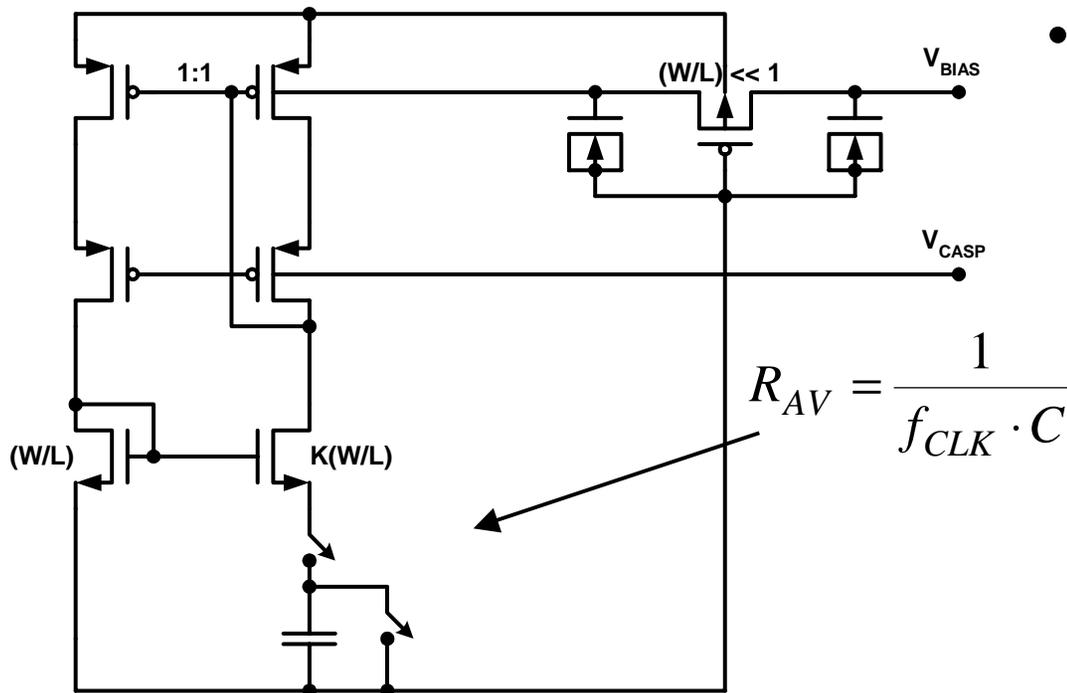




OTA Design – Constant g_m Biasing



- An important limitation of the resistively biased beta-multiplier is that the bias current is first order dependent on the absolute value of a resistor



- Switched capacitor beta-multipliers have two key advantages over their resistive counterparts
 - Absolute accuracy of monolithic capacitors better than resistors
 - Monolithic capacitors have almost zero temperature coefficient





OTA Design – LVCCM Biasing



- Biasing of LVCCMs is very difficult over a wide temperature range because of:
 - Threshold and mobility shift with temperature
 - Constant g_m bias circuits adapt bias current to temperature – thus the LVCCM must remain in saturation over a wide range of currents
 - Most LVCCM bias techniques assume either weak or strong inversion operation, in reality one often wishes to operate in moderate inversion

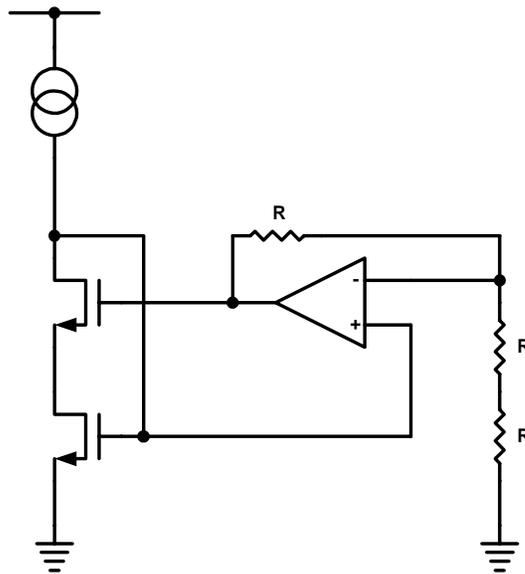




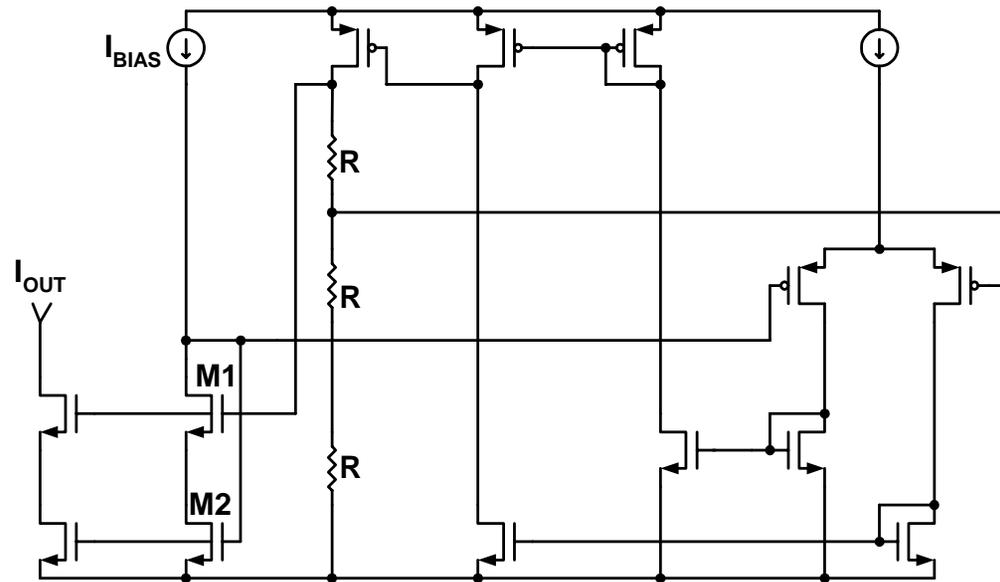
OTA Design – LVCCM Biasing – 1



- The V_{GS} -multiplier is a new LVCCM bias technique developed at UT
- The salient feature of the V_{GS} -multiplier is that it is guaranteed to maximize the V_{DS} on both the top and bottom device in the mirror – independent of bias current, temperature, or any other circuit or environmental characteristics, therefore maximizing r_{out}



V_{GS} -Multiplier Concept



Transistor Level V_{GS} -Multiplier



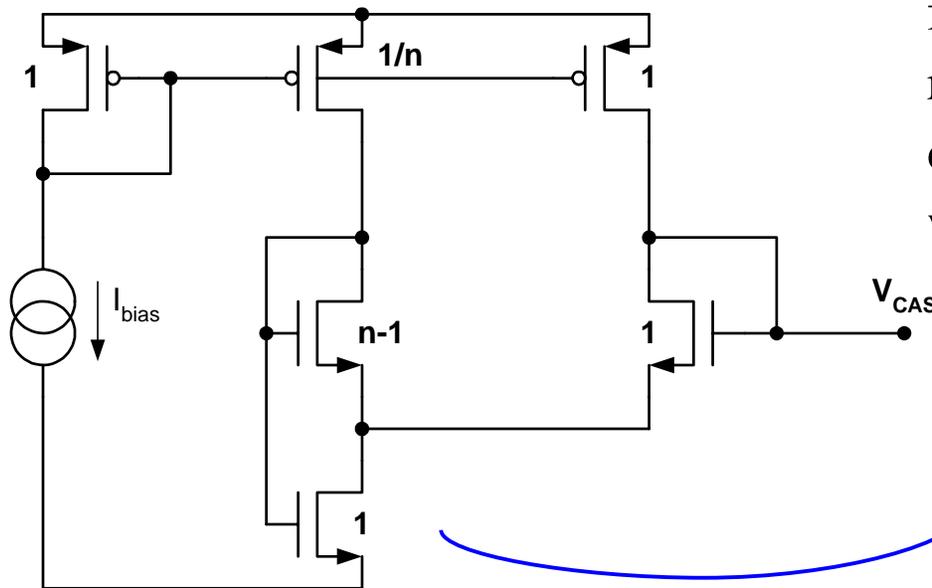


OTA Design – LVCCM Biasing – 2



- Minch¹ recently presented a cascode bias circuit that guarantees maximum output swing at any current level and temperature

- This circuit sets the ratio between the forward (gate & source controlled) and reverse (gate & drain controlled) MOS currents in the bottom-most transistor where $I_D = I_F - I_R$



$$\frac{I_F}{I_R} = n^2$$

¹ B.A. Minch, “A Low-Voltage MOS Cascode Bias Circuit for All Current Levels,” *Proc. IEEE Int. Sym. On Circuits and Systems*, Scottsdale, AZ, 2002, pp. 619 – 622

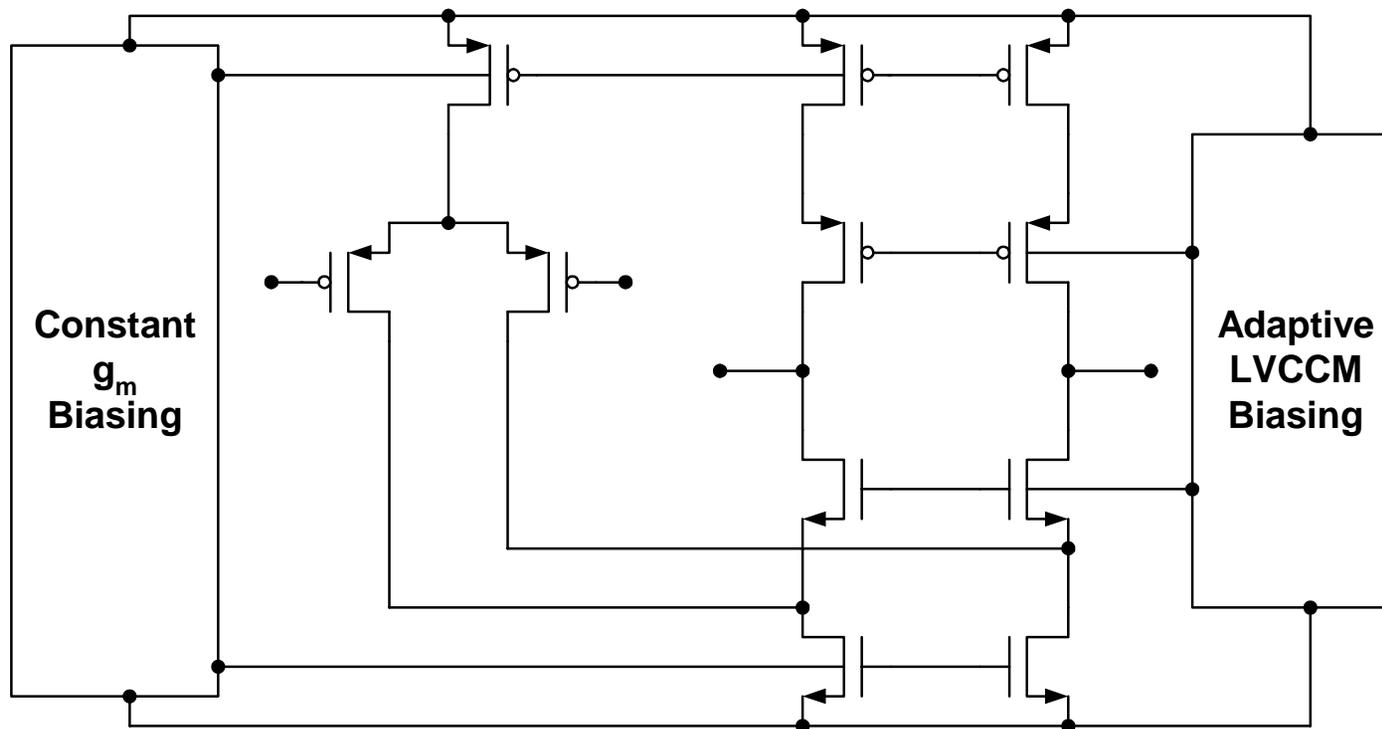




OTA Design – Full Picture



- OTA design showing core OTA, constant g_m biasing, and adaptive LVCCM biasing

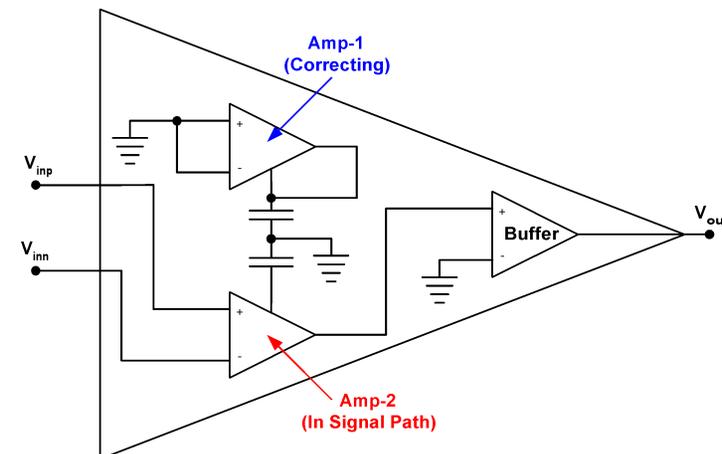
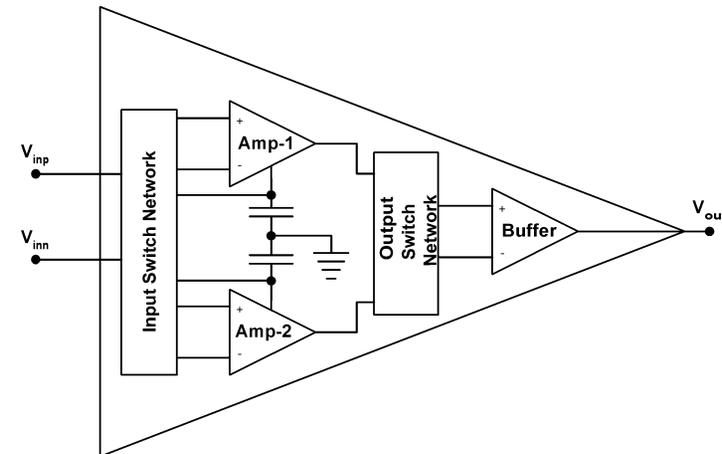




Recent Work – 1/f Noise Reduction



- White noise is reduced at low temperatures, however 1/f noise is only weakly dependent on temperature, therefore the **noise corner will increase with reduced temperature**
- Ping-pong op-amps reduce 1/f noise by using auto-zeroing – thus they can significantly increase dynamic range for systems with a high noise corner

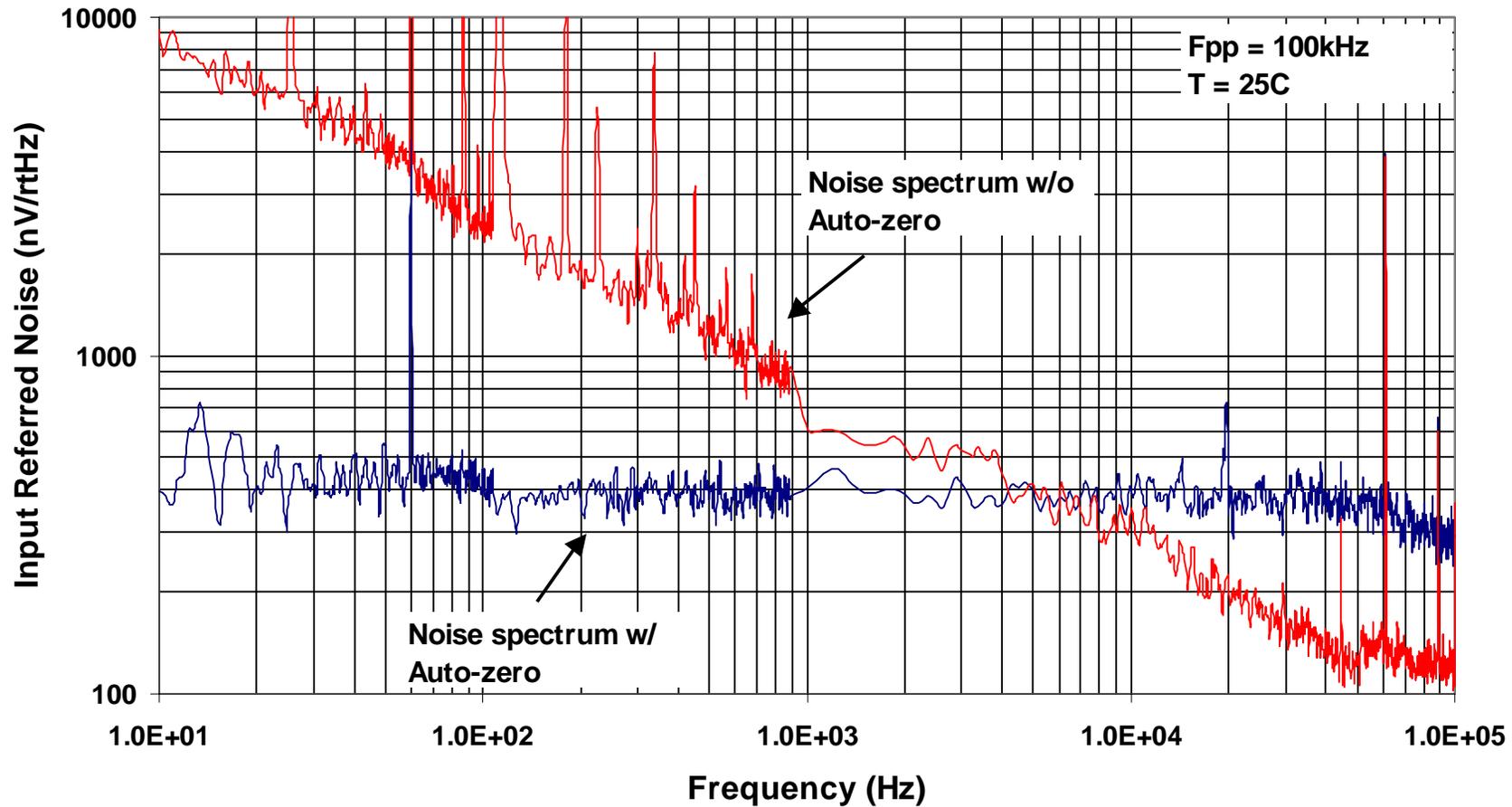




Recent Work – 1/f Noise Reduction



Ping-Pong Op-Amp: Measured Noise Spectrum





Recent Work – 0.35 μ m SOI Op-Amp



- General Purpose Op-Amp in commercially available SOI process:
 - Fabricated in 0.35 μ m/3.3V MOI5 process (commercial/non-radhard)
 - Rail-to-Rail I/O
 - Unity Gain Stable w/ $R_L || C_L = 100k\Omega || 20pF$
 - High current capability (e.g. can drive 5k Ω at 2.5Vpp)
 - Room Temperature Characteristics:

Small-Signal Bandwidth	4 MHz
Unity Gain P.M. ($C_L = 20pF$)	60 degrees
Large-Signal Bandwidth	500 kHz
Thermal Noise Floor	40 nV/rtHz



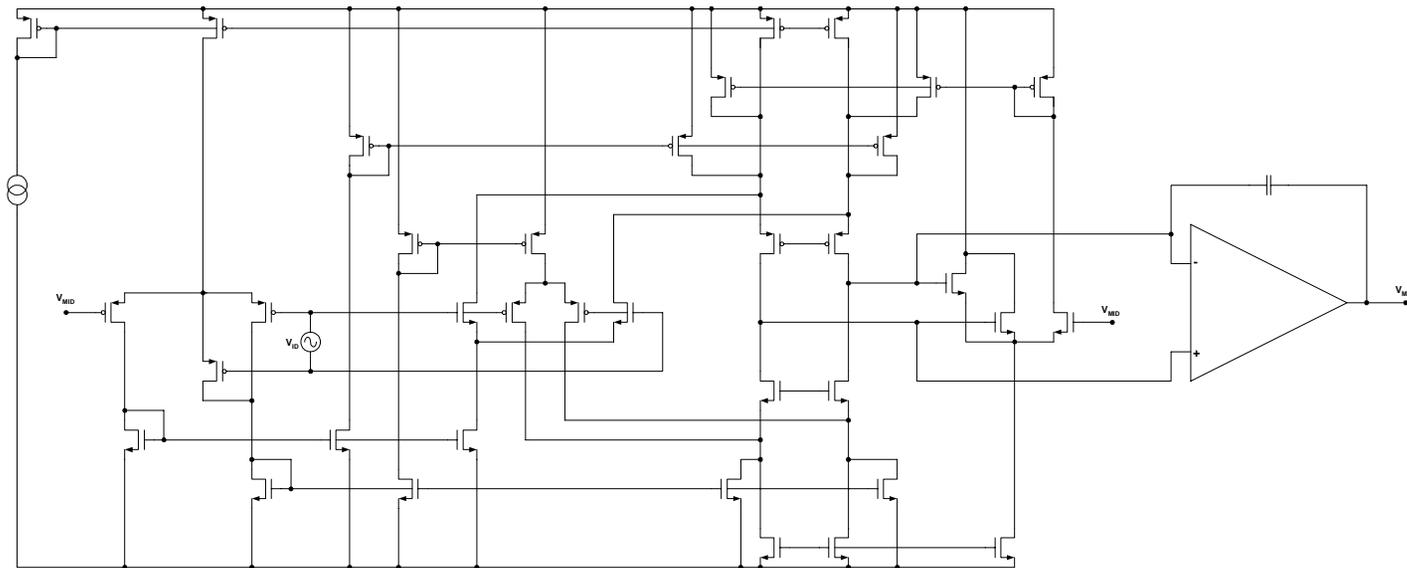


Recent Work – 0.35 μm SOI Op-Amp



- Design Highlights

- 1st stage is fully differential, rail-to-rail ICMR w/ regulated g_m and constant slew rate, CT CMFB
- 2nd stage is a Class-AB driver with low quiescent current for good power efficiency



MOI5 Op-Amp Schematic (LVCCM biasing not shown)

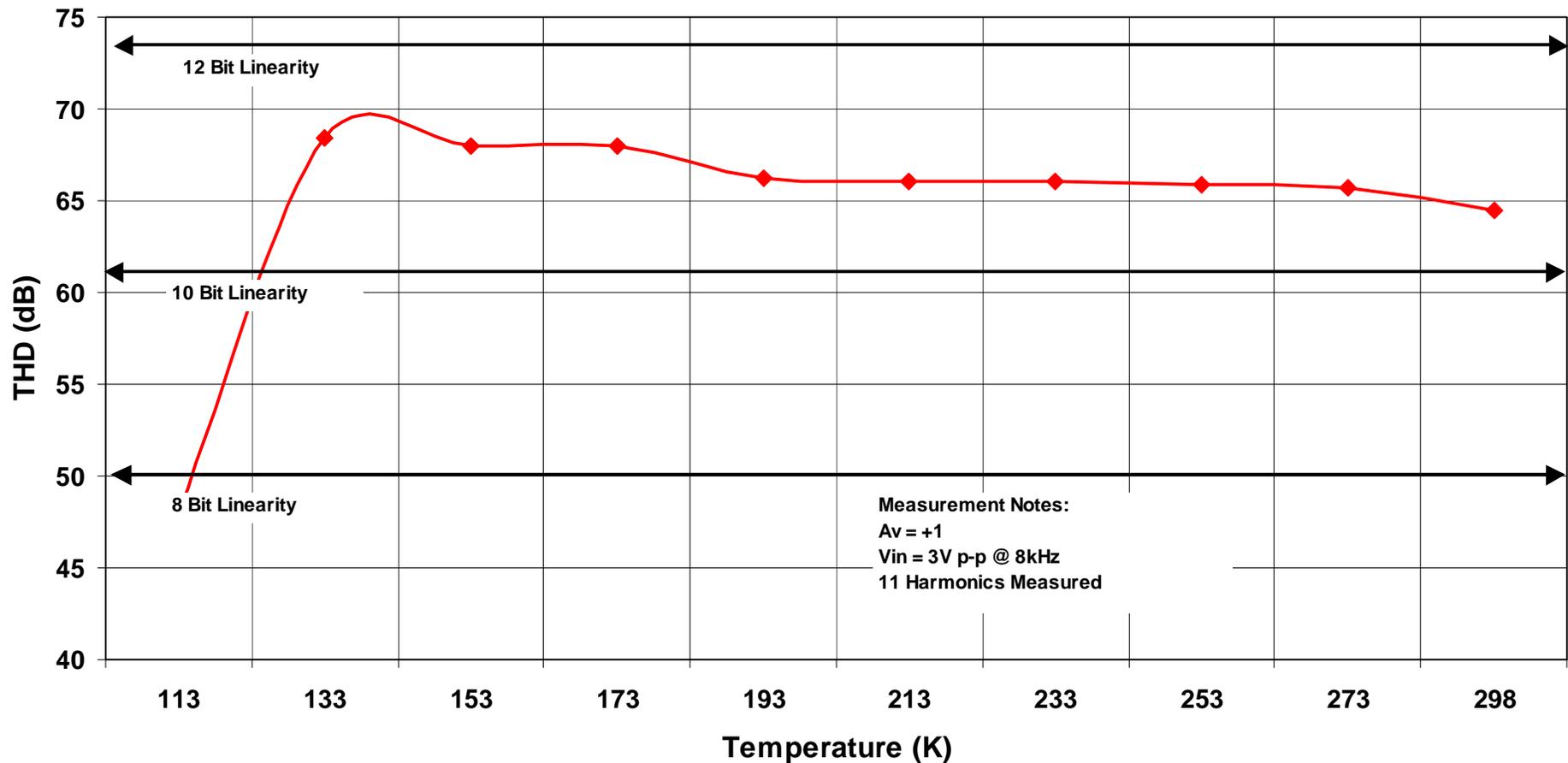




Recent Work – MOI5 Op Amp



MOI5 Op-Amp : Measured THD vs. Temperature





Conclusions



- Low temperature analog CMOS presents challenges and opportunities
- Challenges
 - Modeling
 - Robust design techniques
- Opportunities
 - High bandwidth
 - Reduced power dissipation
 - Reduced thermal noise

